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“Low Noise Amplifier Design for dense phased arrays”

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Abstract

Radio Astronomers demand for highly sensitive astronomical facility. Their demand is a radio telescope that can detect the weakest and deepest radio signal. To fulfill the demand of high sensitive telescope, an entirely new way of realizing a radio telescope is required. One of the most important components in the RF front end that determines the sensitivity of a radio telescope is the Low Noise Amplifier (LNA).

The project has the selected process technologies which was searched and about the different noise matching topologies, input matching topology, wide band noise and input matching topologies has discussed by the author to the requirement of LNA in Astronomical purposes.

In this report, the best process technology candidate was chosen apart from selected technology candidates to obtain the minimum noise temperature over broad range frequency upon the modern era of Astronomical LNAs.

The work was continued to design a single ended LNA to obtain desired transistor parameters while using different noise matching topologies, input matching topologies, wideband noise and input matching topologies to have an LNA achievement with the design goal.

Further two stage amplifier was implemented to obtain minimum noise temperature, good stability, high gain, good input and output reflection coefficient with less power consumption.
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Chapter 1 Low Noise Amplifier design for dense phased arrays

1.1 Introduction

Nowadays Astronomers want to catch the weakest and deepest signals from the sky to reach the real information of the source, the research groups are involved in this work to develop a high sensitivity telescope which could able to catch the weakest signals.

The Netherlands Foundation for Research in Astronomy is currently developing a new radio telescope that is 100 times as sensitive as the best telescopes up to now. This high sensitivity is obtained by increasing the collecting area to approximately 1 square kilometer. The project, entitled Square Kilometer Array (SKA), employs multiple antennas that are connected in a phased array, together forming one larger antenna. The total amount of antennas that are envisioned is approximately 100 million (!).

Besides a large collecting area, a low noise temperature of the entire receiver is of utmost importance. To obtain this low noise temperature, better LNAs than currently available are needed, optimized for application in dense phased arrays.

In the receiver systems the noise properties are mainly determined by the first stage LNA. Noise properties are generally described in terms of the so-called noise parameters.

Both, the noise performance and the input reflection coefficient (S11) of the amplifier depends on the input termination (source/antenna impedance). The source impedance that gives good noise match is mostly different from the source impedance that will give good power match, which makes it difficult to have both good power and noise match simultaneously. Matching becomes even more difficult considering the fact that the antenna impedance (source impedance) is not constant but changes with frequency.

Noise in any receiver is proportional to its physical temperature. Lowering the temperature of the receiver by cooling is one of the methods used to lower the receiver noise. However, phased array concept for 'SKA' employs 100 million antenna elements which means 100 million low noise amplifier following the antenna. Cooling such a large system is not feasible.

Because of huge size of this system, power consumption is also a very important issue. Any increment or reduction in LNA power consumption will be multiplied by 100 million, and it is therefore necessary that the LNA should not consume lot of power.
1.2 Organization of the report

This report have been divided in 6 chapters.

Chapter 2 Introduction to noise.

Chapter 3 Theory of process technologies

Chapter 4 Realization of process technologies.

Chapter 4 Fundamentals of low noise amplifiers.

Chapter 5 Process and results of the work,

Chapter 6 Discussion and Conclusion with Future work.
Chapter 2 Background of noise

In a receiver system, the LNA is usually the active signal processing block after antenna. The power level of the radio astronomy received signal is very weak (below 100dBm).

The LNA should be able of amplifying the signal without causing any significant distortion. Furthermore, the sensitivity of LNA determines the overall receiver sensitivity (Friss Formula). This requires that very little noise from the LNA be introduced to the entire receiver. Another major requirement of the LNA is to provide a large gain to suppress the noise of subsequent blocks.

Noise introduced by the LNA is also a function of source impedance. The optimum source impedance, which results in the minimum noise figure of the LNA, may not be equal to that required by the preceding stage, (usually 50Ω). The result may be an LNA with a good input matching and a poor noise figure or vice versa.

The design of an LNA satisfying all these requirements in a wide bandwidth is even more challenging and needs a careful study of the different parameters affecting noise, gain, and reflection coefficient.

2.1 Noise

In radio observation systems, any signal other than the desired signal is called noise and will reduce the sensitivity of the overall system. Different sources of noise with different noise generation mechanisms exist.

The dominant sources of noise are described as:

- shot noise,
- Flicker noise,
- Thermal noise.

2.1.1 Shot (Schottky) Noise

Shot noise is a white noise current associated with the particulate nature of electrons. In semiconductors, it is related to charge crossing a potential barrier. It is the dominant mechanism in transistors and operational amplifiers at medium and high frequencies [1].

The mean-squared value of shot noise is given by

\[ i_{shi}^2 = 2qI_{dc}\Delta f \]  

(2.1)

Where, 
- \( i_{shi}^2 \) = Shot noise current spectral noise density
- \( q \) = electron charge, \( 1.6 \times 10^{-19} \) Coulombs
- \( I_{dc} \) = DC operating current
- \( \Delta f \) = noise bandwidth
2.1.2. Flicker (1/f) Noise

Flicker noise is associated with combination-recombination of carriers in the emitter-base area of a transistor that are caused by contamination and defects in the silicon lattice structure. This noise type is also called 1/f noise because the amplitude of the noise increases as the frequency decreases [1].

Other components, such as resistors that are made from semi-conducting materials can also exhibit flicker noise. The formula for the mean-squared flicker noise current contains an empirical factor. Different sources give the equation differently; most commonly the expression is given as

\[ i_f^2 = 2qI_{DC}f_c \Delta f \]  

(2.2)

where,

\[ i_f^2 = \text{Flicker noise current spectral density} \]
\[ q = \text{electron charge, } 1.6 \times 10^{-9} \text{ Coulombs} \]
\[ I_{DC} = \text{DC Current} \]
\[ \Delta f = \text{frequency of interest} \]
\[ f_c = \text{Corner frequency} \]
\[ \gamma = \text{an exponent between 1 and 2} \]

2.1.3 Thermal Noise

Thermal noise is caused by the random motion of charges due to the thermal energy the charges receive from their surroundings. The noise frequency is random and has an amplitude that is proportional to the square root of temperature. The frequency component is due to the random motion of the free charges and the amplitude is directly proportional to the temperature. Thermal noise is unaffected by the presence or absence of direct current. All materials with free charges, such as conductors and semiconductors, exhibit thermal noise. In an ohmic resistance, the mean-square open-circuit thermal noise across the resistance is [1]

\[ e_T^2 = 4kTR_0 \Delta f \]  

where

\[ e_T^2 = \text{mean-squared value of Thermal noise voltage} \]
\[ k = \text{Boltzmann’s constant, } 1.38 \times 10^{-23} \text{ Joules/°K} \]
\[ T = \text{Temperature (°K)} \]
\[ \Delta f = \text{frequency range of interest (e.g., amplifier bandwidth)} \]

2.2 Noise in Amplifiers

The most important parameter in determining the performance of a microwave system is the system noise temperature or noise figure. The system noise temperature is almost entirely determined by the first stage amplifier. This chapter derives the general expression for the noise figure in two port network. The expressions for noise parameters for short channel HEMT are reproduced from [2].
2.3 Noise figure of a two port network

One of the main factors that affects the noise figure of an amplifier circuit is the source impedance/admittance, $Y_s = G_s + jB_s$ connected to the input of the amplifier.

![Figure 2.1: Dependence of Noise on Source Impedance](image)

The noise figure of the circuit shown in figure 2.1 is given by equation,

$$F = F_{\text{min}} + \frac{R_n}{G_s} \left[ (G_s - G_{\text{OPT}})^2 + (B_s - B_{\text{OPT}})^2 \right]$$  \hspace{1cm} (2.4)

where,

$F_{\text{min}}$ = minimum value of noise that circuit can have

$Y_{\text{OPT}} = G_{\text{OPT}} + jB_{\text{OPT}}$ is the admittance for which $F = F_{\text{min}}$

$R_n$ is the equivalent noise resistance of the transistor.

The reflection coefficient is related to the admittance by,

$$\Gamma_s = \frac{Y_o - Y_s}{Y_o + Y_s}$$  \hspace{1cm} (2.5)

where, $Y_o$ is the reference admittance for $\Gamma_s$.

Equation 2.4 can be written in terms of source reflection coefficient $\Gamma_s$ and optimal source reflection coefficient $\Gamma_{\text{OPT}}$ as,

$$F = F_{\text{min}} + \frac{R_n |\Gamma_s - \Gamma_{\text{OPT}}|^2}{\left(1 - |\Gamma_s|^2\right)^2 + |\Gamma_{\text{OPT}}|^2}$$  \hspace{1cm} (2.6)

from equation 2.6, it is clear that for better noise performance source impedance should be very close to $\Gamma_{\text{OPT}}$, also the value of $R_n$ should be very low. Low value of $R_n$ gives less dependence of noise figure on the source impedance and hence, source impedance can be considerably different from $\Gamma_{\text{OPT}}$ without much affecting the noise figure.
The noise parameters $\Gamma_{opt}$, $R_s$ and $F_{min}$ depends only on the transistor and are independent of source and load connected. Following section will give a general idea of these noise parameters.

### 2.4 Basic Noise Model

There are many different noise models presented which derives the noise parameters in more detail, Figure 2.2 shows a very simple noise model based on the models presented by [2] and [3].

Figure shows four different noise sources $\bar{e}_g^2$, $\bar{e}_s^2$, $\bar{i}_g^2$ and $\bar{i}_d^2$. The two noise sources $\bar{e}_g^2$ and $\bar{e}_s^2$ represents the noise contribution from the access resistors $R_g$ and $R_s$ respectively and are given by the Nyquist formula,

$$V = \frac{4hfR\Delta f}{\sqrt{e^{hf/kT} - 1}}$$  \hspace{1cm} (2.7)

Figure 2.2: Simplified Noise Model

For $hf/kT = 1$ and which is true for microwave frequencies, $e^{hf/kT} = 1 + hf/kT$, equation 2.7 becomes,

$$V = \sqrt{4kTR\Delta f}$$  \hspace{1cm} (2.8)

thus the noise voltage due to resistances $R_g$ and $R_s$ is,

$$\bar{e}_g^2 = 4kTR_g\Delta f$$  \hspace{1cm} (2.9)

$$\bar{e}_s^2 = 4kTR_s\Delta f$$  \hspace{1cm} (2.10)

Where $k$ is the Boltzmann constant, $T$ is the ambient temperature and $\Delta f$ is the bandwidth.
The two current noise sources \( \overline{i}'_g \) and \( \overline{i}'_d \) represents the channel noise in the intrinsic HEMT.

Figure 2.3 represents the equivalent circuit for figure 2.1 as described in [2], [4] and [5]. Here the four noise sources are replaced by two correlated noise sources preceding the HEMT, which is now considered to be noiseless.

![Diagram of Circuit Representation with Only Two Correlated Noise Sources](image)

**Figure 2.3: Circuit representation with only two correlated noise sources**

In figure 2.3 V’s and I’s are the complex Fourier coefficients of the voltages and currents, and are given as,

\[
\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} + \begin{pmatrix} e_n \\ i_n \end{pmatrix}
\]

As both the noise sources \( e_n \) and \( i_n \) are generated inside the HEMT these noises are correlated and the correlation between these two is given by,

\[
\gamma = \frac{\langle e_n^* i_n \rangle}{\sqrt{\langle e_n^* e_n \rangle \langle i_n^* i_n \rangle}}
\]

(2.12)

the noise current generator can be divided into two parts, \( i_n = i_{n1} + i_{n2} \), where \( i_{n2} \) represents the fraction of \( i_n \) correlated with \( e_n \) and \( i_{n1} \) represents the uncorrelated fraction thus \( \langle i_{n1} i_{n2}^* \rangle = 0 \). This also means that \( i_{n2} \) is proportional to \( e_n \) such that,

\[
i_{n2} = Y_\gamma e_n
\]

(2.13)

\[
\langle i_n^* \rangle = \langle i_{n1}^* \rangle + \langle i_{n2}^* \rangle
\]

(2.14)

\[
\langle e_n i_n^* \rangle = \langle e_n i_{n1}^* \rangle + \langle e_n i_{n2}^* \rangle = \langle e_n i_{n2}^* \rangle
\]

(2.15)

where, the proportionality factor \( Y_\gamma \) is called the correlation admittance. From equation 2.12 and 2.9 we get,

\[
\gamma = \frac{\langle e_n i_{n2}^* \rangle}{\sqrt{\langle e_n^* e_n \rangle \langle i_n^* i_n \rangle}}
\]

(2.16)
\[ \gamma^2 = \frac{\langle |i_n|^2 \rangle}{|i_e|^2} \]  

(2.17)

and from equation 2.10 and 2.13 we get,

\[ Y_e^2 = \gamma \sqrt{\frac{\langle |i_n|^2 \rangle}{\langle |e_n|^2 \rangle}} \]  

(2.19)

and so,

\[ Y_e = G_{\gamma} + jB_{\gamma} \]  

(2.20)

\[ Y_e = \text{Re} [\gamma] \sqrt{\frac{\langle |i_n|^2 \rangle}{\langle |e_n|^2 \rangle}} - j \text{Im} [\gamma] \sqrt{\frac{\langle |i_n|^2 \rangle}{\langle |e_n|^2 \rangle}} \]  

(2.21)

next, we replace the noise voltage and current source with \( R_n \) and \( G_n \) as shown in figure 2.4, where \( Y_e \) is noise free, which is represented by the noise temperature of 0 K. Values of \( R_n \) and \( G_n \) are given by equation 2.18 and 2.19.

\[ \left( \begin{array}{c} e_{kTR} \Delta f V \\ i_{kTG} \Delta f A \end{array} \right) \]  

(2.22)

\[ \left( \begin{array}{c} \langle |i_n|^2 \rangle \\ \langle |e_n|^2 \rangle \end{array} \right) = 4kTR_n \Delta f \left[ V^2 \right] \]  

(2.23)

The noise figure of this circuit can now be determined using the well known equation 2.20

\[ F_e = 1 + \frac{T_e}{T_0} \]  

(2.24)

where, \( T_e \) is the equivalent noise temperature of the HEMT and \( T_0 \) is the noise temperature of the source. The ratio \( T_e/T_0 \) is determined by calculating the noise power densities from the source and from the HEMT by finding the short circuit current at the output from each of the noise source \( G_s \), \( R_s \) and \( G_s \), thus we get,

\[ KT_e G = \frac{\langle i_{GS}^2 \rangle}{4(G_{s}G_{s} + G_{s}G_{s} - G_{s}G_{s})} \Delta f \]  

(2.25)
\[ K T \gamma G = \frac{\left\langle i_{Gn}^2 \right\rangle + \left\langle i_{Rn}^2 \right\rangle}{4 \left( G_n + G_{Rn} - G_{\gamma} \right) \Delta f} \]  

(2.26)

where, \( i \) and G is the gain of the HEMT. From equation 2.20, 2.21 and 2.22 we get,

\[ F_s = \frac{\left\langle i_{GS}^2 \right\rangle + \left\langle i_{Rn}^2 \right\rangle + \left\langle i_{Rn}^2 \right\rangle}{\left\langle i_{GS}^2 \right\rangle} \]  

(2.27)

\[ F_s = 1 + \frac{1}{G_s} \left( G_n + R_n \left| Y_s + Y_s \right|^2 \right) \]  

(2.28)

From equation 2.24 it can be seen that the noise figure depends on the source. To examine the dependence of noise figure on the source impedance equation 2.24 can be written as,

\[ \left[ G_s - \left( \frac{F_s - 1}{2R_n} - G_{\gamma} \right) \right]^2 + \left[ B_s - (-B_s) \right]^2 = \frac{(F_s - 1)}{4R_n} - \frac{(F_s - 1)}{R_n} - \frac{G_n}{R_n} \]  

(2.29)

2.25 represent the equation of the constant \( F \) circle in the source admittance plane, with its center at

\[ (G_s, B_s) = \left( \frac{F_s - 1}{2R_n} - G_{\gamma} - B_{\gamma} \right) \]  

(2.30)

and with radius,

\[ R_{noisecircle} = \sqrt{(F_s - 1)^2 - \frac{G_n}{R_n} \left( \frac{G_{\gamma}}{R_n} \right)^2} \]  

(2.31)

there are two roots for \( F_s \) which represents two extremities for \( F_s \), \( F_{\text{min}} \) given by 2.28 and \( F_{\text{max}} \), the expression for \( F_{\text{min}} \) is given as,

\[ F_{\text{min}} = 1 + 2 \left( R_n G_s + \sqrt{R_n G_n + (R_n G_{\gamma})^2} \right) \]  

(2.32)

For

\[ Y_{OPT} = \frac{G_n}{R_n} + G_{\gamma} - jB_{\gamma} \]  

(2.33)

When values of \( F_{\text{min}}, Y_{OPT} \) and \( R_n \) are used as noise parameters we get,

\[ F = F_{\text{min}} + \frac{R_n}{G_s} \left| Y_s - Y_{OPT} \right|^2 \]  

(2.34)

thus we arrive to the equation 2.1.

**2.5 Intrinsic Noise Sources**

The channel noise \( i_s \) and \( i_d \) in figure 2.2 arises from the carrier velocity fluctuation in the channel due to scattering. In case of n type of material, the main cause of the scattering in the channel is the collision of free electron with an ionized doping.
impurity. As described by Alain Cappy [2], the drain noise sources can be expressed as,

\[ \bar{i}_d^2 = 4kTg_m P \Delta f \]

where \( P \) is given by,

\[ P = \frac{I_	ext{ds}}{E_L g_m} \]

the gate noise current source is given by,

\[ \bar{i}_g^2 = 4kT \Delta f \frac{C_w^2}{g_m} R \]

where, parameter \( R \) depends on the bias conditions. If the influence of \( C_{gd} \) is neglected then the noise parameters can be expressed as,

\[ F_{\text{min}} = 1 + 2\sqrt{P + R - 2C \sqrt{PR} \cdot \frac{f}{f_c}} \sqrt{g_m(R_s + R_g) + \frac{PR(1 - C^2)}{P + R - 2C \sqrt{PR}}} \]

\[ Z_{\text{opt}} = \sqrt{g_m(R_s + R_g) + \frac{PR(1 - C^2)}{P + R - 2C \sqrt{PR}}} \cdot \frac{1}{C_{gs} + \frac{1}{C_{gs}^2} \left( \frac{P - C \sqrt{PR}}{P + R - 2C \sqrt{PR}} \right)} \]

\[ g_m = g_m \left( \frac{f}{f_c} \right)^2 \sqrt{P + R - 2C \sqrt{PR}} \]

where, \( C_{gs} \) is the gate to source capacitance,

\[ f_c = \frac{g_m}{2\pi C_{gs}} \] is the cut off frequency,

\( f \) is the operating frequency, and

\( C \) is the correlation coefficient of the correlated gate and drain noise.

It can be seen from equation 2.34 that the noise figure increases linearly with frequency, and varies inversely with the cut off frequency. Also, the drain noise and gate noise has same origin and hence they are partly correlated, therefore the correlation between drain noise and gate noise is subtracted from the noise figure. This is one of the reason that HEMT’s are low noise devices, other reason is that HEMT’s have higher transconductance which gives lower value of \( \bar{i}_g^2 \) in equation 2.33.

2.6 Noise figure

Noise figure: Noise figure (NF) is a measure of signal-to-noise ratio (SNR) degradation as the signal through the receiver front-end. Mathematically, NF is defined as the ratio of the input SNR to the output SNR of the system.
**Noise Figure (NF)** may be defined for each block as well as the entire receiver. \( NF_{LNA} \), for instance, determines the inherent noise of the LNA, which is added to the signal through the amplification process.

### 2.7 System Level Noise Figure Considerations

In a receiver path, as the signal propagates from the antenna to digital part, different blocks may introduce noise to the signal. The overall NF of the receiver depends on the NF of each block as well as the gain of preceding stages. Intuitively, larger signals are less susceptible to noise, and this is why the large gain of one stage makes the noise of the following stage less important.

**Friis Formula** shows that the overall NF of a cascaded system is given by:

\[
NF_{tot} = NF_1 + \frac{NF_2 - 1}{A_1} + \frac{NF_3 - 1}{A_1A_2} + \ldots
\]  

(2.41)

Noise figure in terms of noise temperature:

\[
NF = T_e + \frac{T_0}{T_0}
\]

(2.42)

Where \( T_e = (NF - 1) \)

Where \( NF_i \) and \( A_i \) are the noise figure and available power gain of each stage, respectively. Assuming that \( A_i \) is a large value then \( NF_i \) is the dominant term in. This accounts for the fact that the low noise of the LNA, i.e., low \( NF_i \), is of great importance in the receiver design. Note that \( NF_2 \) is the NF of the second stage, it is essential that the gain of the LNA be large enough (high \( A_1 \)) to reduce the contribution of \( NF_2 \) to \( NF_{tot} \). \( NF_{tot} \) determines the sensitivity of the overall receiver.
Chapter 3 Study on Process Technologies

There are many technologies available in integrated circuit fabrication nowadays. Among them, BJT (Bipolar Junction Transistors), MOSFET (Metal-Oxide-Semiconductor Field Effect Transistors) (i.e., CMOS), BiCMOS (i.e., SiGe), MESFET (Metal-Semiconductor Field Effect Transistors) (i.e., GaAs), HBT (Heterojunction Bipolar Transistors) (i.e., SiGe, GaAs, etc), and HEMT (High Electron Mobility Transistors) (i.e., GaAs, InP, GaN, etc) are among the mature technology processes [7][8].

3.1 Comparison of Technologies

The choice of technology for RF application is mainly based on four issues: performance, wafer cost, level of integration and time to market [7]. Among these four, performance is of utmost importance in our case as a rather low noise figure is required. Here, three prevalent technologies, i.e. GaAs, Si, SiGe are discussed.

Both bipolar and FET devices are used in high-frequency amplifiers. Homojunction bipolar devices and silicon FET devices are generally suitable for use at frequencies up to a few gigahertz; some advanced technologies, especially short-gate silicon MOS devices, may be useful well in to the microwave or even millimeter regions. The minimum noise figures of devices realized in III-V technologies are significantly lower than those in silicon, however. This is especially true of high-electron-mobility transistors (HEMTs) and pseudomorphic HEMTs, sometimes called pHEMTs. These offer extraordinarily low noise figures. The most advanced pHEMT technologies can operate into the high end of the millimeter-wave region. Heterojunction bipolar devices (HBTs) are also used at microwave frequencies. Their noise figures are inferior to FETs, however, so they are used primarily for low-distortion and large-signal operation [9].

At this writing, HEMT devices have almost completely supplanted conventional GaAs MESFETs for low-noise microwave applications. The higher electron mobility in HEMTs, combined with process optimization to reduce resistive parasitics, is largely responsible for their low noise figures. This advantage comes at a cost: HEMT devices operate at very low currents, giving them, at best, and limited ability to handle large signals. They also exhibit a stronger transconductance nonlinearity, giving them higher levels of distortion than conventional MESFETs[9].

3.1.1 GaAs Technology

GaAs MESFETs or pHEMTs are usually used in the applications close to the antenna, which require high performance [7]. E-pHEMT also have developed for low noise applications [14] Noise and linearity are considered as the most important performance parameters in GaAs technology.

According to Table.1.1, the electron mobility of GaAs is much larger than that of Silicon technology, which means that devices of GaAs can operate at higher speeds and are suitable for high frequency usage [7][10].
Table 1.1 Comparison of properties of Si and GaAs technology (extracted from [7])

<table>
<thead>
<tr>
<th>Properties</th>
<th>Silicon</th>
<th>GaAs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Breakdown Field (V/cm)</td>
<td>$\approx 3 \times 10^3$</td>
<td>$\approx 4 \times 10^5$</td>
</tr>
<tr>
<td>Electron Mobility (cm$^2$/V·sec)</td>
<td>$\approx 1500$</td>
<td>$\approx 8500$</td>
</tr>
<tr>
<td>Thermal Conductivity at 300K (watt/cm$^2$·K)</td>
<td>$\approx 1.45$</td>
<td>$\approx 0.45$</td>
</tr>
<tr>
<td>Saturated Electron Drift Velocity (@10$^5$V/cm)</td>
<td>$\approx 10^7$</td>
<td>$\approx 10^7$</td>
</tr>
<tr>
<td>1/f Noise Corner Frequency (Hz)</td>
<td>BJT/HBT</td>
<td>MOSFET/MESFET</td>
</tr>
<tr>
<td>Substrate Resistivity (typical) (Ω·cm)</td>
<td>$\approx 10^9$</td>
<td>$\approx 10^9$</td>
</tr>
</tbody>
</table>

In the same table, the substrate resistivity of GaAs is much larger than that of Silicon. This semi-insulating nature of substrate results in less parasitic coupling and better circuit-circuit isolation. In the aspect of passive components, this highly resistive substrate provides a high quality factor (Q).

The ohmic resistances leading to the device, which play a key role in determining noise figure, are dominated by low-field electron mobility and the gate resistance. Compared to Si based technology, GaAs has a higher low-field mobility, thus lower noise. The metal-gate structure of GaAs MESFET or PHEMT also reduces the series gate resistance compared to the silicided MOSFET gate. Therefore, GaAs is better in the sense of noise. When the linearity is considered, GaAs MESFET or PHEMT is also expected to be better than Silicon bipolar devices due to the square-law of current to voltage relation.

The disadvantages of GaAs are its low yield and high cost, compared to most silicon-based technologies.

3.1.2 Silicon-based Technology

Silicon-based technologies such as CMOS and BiCMOS, are regarded as cheaper process compared to other semi-conductor based technologies, eg. GaAs and SiGe. This is because processes for CMOS and BiCMOS circuits provide higher yields (fewer defects per wafer). Meanwhile, the high volume of orders enjoyed by CMOS fabrication facilities helps reduce the cost of such circuits through economies of scale. In addition, analog circuits implemented in CMOS can be easily integrated on the same substrate with the digital base-band processing circuits for a truly optimal single chip implementation of the system [10].

Traditionally, Si-based technologies are not suitable for high frequency (RF) application owing to their lower transistor cut-off frequencies. However, the development in recent years shows that, Si-based circuits, first bipolar and then MOS have attained similar $f_t$’s which makes them suitable for operation in the frequency of tens of GHz. [7] [10] [11].

However, the disadvantages of Si-based technologies are apparent. First, though the silicon devices are expected to operate at high frequency, its performance is
generally achieved at higher power dissipation levels and lower gains than GaAs devices [4]. Second, the substrate loss and inter-device isolation need to be improved for RF applications. Several methods are presented in [13], such as resistivity increasing, “guard rings”, “triple-well” technology etc.

3.1.3 SiGe Technology

SiGe process technology has become a key technology in the recent years. The SiGe BiCMOS technology provides high-performance SiGe heterojunction bipolar transistors (HBTs) combined with CMOS technology. The cut-off frequency of the SiGe HBTs can exceed 200GHz, which is very attractive in RF area. The problem of base resistance, which used to be the obstacle of low noise applications, has been improved by aggressive lateral scaling and advanced processing techniques, such as carbon doped base layer [14] [11]. The base resistance is significantly reduced in this way. Compared to the FET, the SiGe HBT has an exponential relationship between output current and input voltage, which makes it achieve about three times the transconductance, and thus three times the drive capability, of a FET [11].

Due to the same low-resistivity substrate as silicon technology, RF loss and quality factor of passive components should be paid attention to.

The choice of process technology is driven by the desire to simultaneously meet objectives for speed, noise, linearity, gain, low power dissipation, yield and efficiency. None of the technology can satisfy all of these requirements at RF, IF and baseband. In the baseband region, Si CMOS is the dominant technology. IF circuits such as mixers can be realized in a mix of CMOS, BiCMOS and Bipolar technologies. In the RF arena, the circuits such as power amplifier and LNA are generally realized in GaAs. [10]

3.2 Noise Model of Transistor

There are two types of noise model of transistors, bipolar and FET. The noise model of bipolar transistor is illustrated in Fig.3.1.

![Figure3.1: Noise model of a bipolar transistor](image)

In the figure, \(i_b\) and \(i_c\) are shot noise sources introduced by the diffusion current \(I_c\) and \(I_b\). \(i_{bf}\) is the 1/f noise source, which is mostly negligible. \(V_{n,b}\) is the noise of base resistance, which contributes most noise in a bipolar transistor. Noise model of the FET are shown in Fig.3.2, where the principle cause of noise is the thermal noise produced by the drain-source channel resistance, denoted as \(i_d\). \(V_{n,g}\) is the noise source of gate resistance, which is usually very small due to the metal gate. \(i_{df}\) is the 1/f noise that comes from defects and traps. \(i_g\) is the shot noise that only exists in the JFET. \(i_{ig}\) is the gate induced noise introduced by capacitive coupling, which is noticeable at very high frequencies.
3.3 Conclusions

In this chapter, we discussed some issues on the process technologies. In order to draw a clear image of the noise origin for the active part (i.e. discrete transistor), three different technologies were studied. The comparison of the features gave the appropriate application area for each technology, which is regarded as the guidance of choosing a technology in our case. According to the comparison Si based process based technology CMOS also offering low noise figures, which is not open in the markets bounded by foundry. But GaAs seems to be the most suitable technology since it is widely used in the front end of RF system.

3.4 High Electron Mobility Transistor

This chapter describes the basic operation of HEMT (High Electron mobility transistor). Starting with the basic structure of GaAs based HEMT and basic working principle. To consider the power consumption of the amplifier, expressions for large signal drain current and transconductance are reproduced from [15].

3.4.1 HEMT Structure

In High Electron Mobility Transistors, a wide band gap doped n-type material is places over a narrow band gap un-doped material, and a thin metal layer is deposited over the doped n-type material forming a Schottky Barrier Junction. The resulting band diagram for a depletion type device under zero bias condition is shown in figure 3.3. This structure creates a potential well over a very thin region at the boundary of two materials, which results in large electron concentration in narrow region along un-doped InAlAs side. Because of the high concentration of the carrier occurring over very thin region, it is called as two-dimensional electron gas (2-DEG).

Figure 3.4 shows the cross sectional view of a HEMT. Generally, in depletion type of transistor, under zero gate bias condition the transistor conducts through the 2-DEG region [15]. Now, if an external voltage is applied across the drain-source terminals, the electrons in this un-doped or lightly doped semiconductor material will travel with very high speed across the channel. This is because the electrons do not encounter, and scattered by, any ionized donor atoms.

The density of free electrons in 2-DEG region is controlled by the gate voltage. In depletion type of device, increasing the negative voltage at gate decreases the depth of potential well in figure 3.3, which reduces the free electron density. There are two most important gate voltages which should be considered in order to describe the
device large signal behavior, critical gate voltage (VGC) given by equation 3.1 and the turn off voltage (Voff) given by equation 3.2

\[ V_{GC} = \frac{q(d + d_0)n_{s0}}{\varepsilon} + V_{off} + E_{F(n_{s0})} \]  
(3.1)
\[ V_{off} = V_{hi} - V_{p2} - \Delta E_c \]  
(3.2)
\[ V_{p2} = \frac{qN_d d^2}{2\varepsilon} \]  
(3.3)

where,

- q is the electron charge
- \( n_{s0} \) is the maximum sheet density
- \( E_{F(n_{s0})} \) is the Fermi level at maximum sheet density

\[ E \] is the dielectric constant of the material
\( N_d \) is the donor density in n type InAlAs layer, and
\( V_{p2} \) is the pinch off voltage given by equation 2.3

The critical gate voltage is a gate voltage, at which the electron concentration in the 2-DEG region reaches the maximum possible sheet density \( n_{s0} \), and the turn off voltage is a gate voltage at which the 2-DEG layer no longer exists and HEMT acts like normal MESFET with further increase in gate bias.

### 3.4.2 HEMT Large Signal Model

Here, the complete large signal behavior of HEMT is not described, but the expressions for drain current, and transconductance are reproduced from [15], to consider the effect of channel length and width on drain current and transconductance. Under linear region of operation when \( V_{gs} < V_{GC} \),
\[ I_{DS0} = \frac{\mu_0 Z e^2}{(\varepsilon_L + V_{ds})(d + d_0)} \left\{ V_{G1}V_{ds} + \frac{CV_{ds}}{2} - \frac{V_{ds}^2}{2} + \frac{2(D - CV_{ds})^{3/2} - D^{3/2}}{3C} \right\} \] (3.4)

\[ G_{m0} = \frac{\mu_0 Z e^2}{(\varepsilon_L + V_{ds})(d + d_0)} \left( V_{ds} + \left( D - CV_{ds} \right)^{1/2} - D^{1/2} \right) \] (3.5)

Like the MOSFET, HEMT's also suffers from gate length modulation. The effect of gate length modulation is considered in equation 3.6 and 3.7, the gate length modulation results in increase of drain-source current.

\[ I_{ds} = I_{DS0} \left( 1 + \Lambda V_{ds} \right) \] (3.6)

\[ g_m = G_{m0} \left( 1 + \Lambda V_{ds} \right) \] (3.7)

\[ \text{Figure 3.4: Cross sectional of conventional HEMT} \]

VG1, C and D in equation 3.4 and 3.5 are given as [2],

\[ V_{G1} = V_{gs} - V_{OFF} - K_1 \] (3.8)

\[ C = \frac{\varepsilon K_2^2}{q(d + d_0)} \] (3.9)

\[ D = \frac{C^2}{4} + CV_{G1} + K_2^2 K_3 \] (3.10)

The parameters K1, K2 and K3 are the process dependant constants.
Chapter 4 Realization of process technologies

In this chapter process technology based discrete transistors are realized, first starting with different process technology based candidates and secondly with same process technology based candidates were compared to obtain minimum noise figure and low noise resistance and low optimum impedance.

4.1 Comparison of different process technology based candidates

Several transistors are discussed and compared below starting with Si, SiGe, GaAs process based candidates.

4.1.1 Si Process technology

This process technology offered by different foundries and looking on several foundries to get the Si made transistors show the minimum noise figure and low noise resistance and low optimum reflection coefficient.

This process based technologies were studied carefully to choose best noise parameters.

Si based process technology Bipolar transistor is AT41511 NPN BJT which only offering minimum noise figure amongst other Si Based process technologies are available and other parameters noise resistance and optimum reflection coefficient are also has studied [14].

4.1.2 SiGe Process Technology

The SiGe based process technology transistors have searched to get good noise parameters of the transistor to achieve best low noise amplifier.

SiGe based process technology candidate BFP740F SiGe-NPN RF-Transistor from Infineon Technologies which is only offering minimum noise figure amongst other SiGe process technologies based transistors are available and other parameters noise resistance and optimum reflection coefficient are also has studied [16].

4.1.3 GaAs process based technology of HJ FET from NEC

GaAs processed based technology, California Eastern Laboratories (NEC CEL) offering NE 3510M04 HJ FET transistor which is showing typical low noise behavior [17].

4.1.4 GaAs process technology of pHEMT from Avago

ATF-35143 pHEMT Transistor which is based on GaAs process technology, this transistor producing company name was Agilent now has changed to Avago technologies [14]. This process transistor is offering lowest minimum noise figure.
4.1.5 GaAs process technology of EpHEMT from avago

ATF-58143 EpHEMT Transistor which is based on GaAs process technology, this transistor producing company name was Agilent now changed to Avago technologies [14]. This process transistor is offering lowest minimum noise figure.

4.2 Comparison of different process technology based transistors noise parameters as a function of frequency

Here, all the process technology based transistors are compared together to have a best transistor noise parameters as a function of frequency, keeping the current and voltage as a constant.

As we discussed above the processes Si, SiGe, GaAs based transistors.

1) Si process technology based transistor AT-41511 BJT 2.7V, 5mA.
2) SiGe process technology based transistor BFP740F SiGe-NPN BJT 2V, 10mA.
3) GaAs process technology based transistor NE3510M04 HJ FET 2V, 10mA.
4) GaAs process technology based transistor ATF 58143 E-pHEMT 3V, 30mA.
5) GaAs process technology based transistor ATF 35143 pHEMT 2V, 10mA.

4.2.1 Minimum noise figure as a function of frequency

Here the comparison was taken in to account on minimum noise figure as a function of frequency, keeping the voltage and current as constant.

The diagram which is showing below comparison of process technology based transistors noise parameter is minimum noise figure as a function of frequency.

![Minimum Noise Figure verses Frequency](image)

Figure 4.1: Fmin vs Frequency of different process transistors

The above Figure 4.1 explains, how the behavior of different processes.
1) Si process technology based transistor AT-41511 BJT 2.7V, 5mA, which is showing highest minimum noise figure (Fmin) behavior compared to all other transistors, exhibiting Fmin value is 1.05 dB at 1GHz, lower frequencies and at higher frequencies greatly increasing as a function of frequency.

2) SiGe process technology based transistor BFP740F SiGe-NPN BJT, which is showing minimum noise figure (Fmin) value of 0.37dB at 1 GHz frequency and increasing linearly as a function of frequency. This value is quite lower than above 1st process candidate.

3) GaAs process technology based transistor NE3510M04 HJ FET, which is showing lowest minimum noise figure (Fmin) behavior compared to above two process transistors. Fmin value is 0.27 dB at 1 GHz frequency and slowly increasing for higher frequencies but the behavior is showing flatness compared to all other transistors.

4) GaAs process technology based transistor ATF 58143 E-pHEMT, which is showing lower minimum noise figure (Fmin) behavior compared to above three process transistors. Fmin value is 0.2 dB at 1 GHz frequency and increasing linearly for higher frequencies.

5) GaAs process technology based transistor ATF 35143 pHEMT which is showing lowest minimum noise figure (Fmin) behavior compared to above four process transistors. Fmin value is 0.12 dB at 1 GHz frequency and increasing linearly for higher frequencies.

4.2.2 Conclusion
Compared to all process candidates, ATF-35143 pHEMT is the best candidate which is offering lowest minimum noise figure of 0.12 dB at 1GHz frequency and NE3510M04 HJ FET is offering flatness over broad range of frequencies as a function of frequencies.

4.2.3 Optimum reflection coefficient (Gamma opt) in magnitude as a function of frequency

Here, the comparison was taken in to account on optimum reflection coefficient (magnitude) as a function of frequency, keeping the voltage and current as constant.

The diagram which is showing below comparison of process technology based transistors Gamma opt (magnitude) as a function of frequency.
The above Figure 4.2 explains, how the behavior of different processes.

1) Si process technology based transistor AT-41511 BJT 2.7V, 5mA, which is showing lowest optimum reflection coefficient (Gamma opt) behavior compared to 1, 4, 5 process transistors. Gamma opt value is 0.38 in magnitude at 1GHz frequency, decreasing linearly up to frequencies of 2GHz and increasing linearly for higher frequencies as a function of frequency.

2) SiGe process technology based transistor BFP740F SiGe-NPN BJT, which is showing low optimum reflection coefficient (Gamma opt) behavior compared to all four process transistors. Gamma opt value is 0.25 in magnitude at 1GHz frequency, decreasing linearly up to frequencies of 2GHz and increasing linearly taking a shape of ripple for higher frequencies as a function of frequency.

3) GaAs process technology based transistor NE3510MO4 HJ FET, which is showing high optimum reflection coefficient (Gamma opt) behavior compared to all 4 process transistors. Gamma opt value is 0.898 in magnitude at 1GHz frequency, decreasing linearly for higher frequencies as a function of frequency.

4) GaAs process technology based transistor ATF 58143 EpHEMT, which is showing low optimum reflection coefficient (Gamma opt) behavior compared to all four process transistors. Gamma opt value is 0.36 in magnitude at 1GHz frequency, decreasing linearly up to frequencies of 2GHz and increasing linearly for higher frequencies as a function of frequency.

5) GaAs process technology based transistor ATF 35143 which is showing low optimum reflection coefficient (Gamma opt) behavior compared to 1st process transistor. Gamma opt value is 0.87 in magnitude at 1GHz frequency, decreasing linearly for higher frequencies as a function of frequency.

4.2.4 Conclusion

Compared to all different process candidates, SiGe process technology based transistor BFP740F SiGe-NPN BJT offering the lowest optimum reflection coefficient

---

**Figure 4.2: Gamma opt vs Frequency of different process transistors**

![Optimum Reflection Coefficient verses Frequency](image)
(Gamma opt) value is 0.25 in magnitude at 1GHz frequency and this transistor can be useful for broad frequency range of our interest.

### 4.2.5 Noise resistance (Rn) as a function of frequency

Here the comparison on noise parameter as a function of frequency, keeping the voltage and current constant.

The diagram which is showing below comparison of different process technology based transistors noise resistance (Rn) as a function of frequency.

![Noise Resistance Vs Frequency](image)

**Figure 4.3: Rn vs Frequency of different process transistors**

The above Figure 4.3 explains, how the behavior of different processes.

1) Si process technology based transistor AT-41511 BJT 2.7V, 5mA, which is showing low noise resistance (Rn) behavior compared to 3rd process transistor. Gamma opt value is 0.18 at 1GHz frequency, decreasing linearly for higher frequencies as a function of frequency.

2) SiGe process technology based transistor BFP740F SiGe-NPN BJT, which is showing low optimum reflection coefficient (Gamma opt) behavior compared to 1, 3, 5 process transistors. Gamma opt value is 0.12 at 1GHz frequency, decreasing linearly up to frequencies of less than 2GHz and showing flatness up to some higher frequencies as a function of frequency.

3) GaAs process technology based transistor NE3510M04 HJ FET, which is showing high noise resistance (Rn) behavior compared to all 4 process transistors. Rn value is 0.28 at 1GHz frequency, decreasing linearly for higher frequencies as a function of frequency.

4) GaAs process technology based transistor ATF 58143 E-pHEMT, which is showing low noise resistance (Rn) behavior compared to all four process transistors. Rn value is 0.04 at 1GHz frequency, showing flatness up to 2GHz frequency and increasing linearly for higher frequencies as a function of frequency.
5) GaAs process technology based transistor ATF 35143 which is showing low noise resistance (Rn) behavior compared to 1, 2 process transistors. Rn value is 0.15 at 1GHz frequency, showing flatness up to 1.8GHz frequency and increasing linearly for higher frequencies as a function of frequency.

4.2.6 Conclusion

Compared to all different process candidates, GaAs E-pHEMT process candidate ATF 58143 E-pHEMT 3V, 30m.A. showing low noise resistance value of 0.04 for a broad frequency range.

4.2.7 Over all conclusion of different process based transistors

In all different process transistors pHEMT and E-pHEMT processes are giving lower minimum noise figures, first we will look at one of the noise parameter of transistor is minimum noise figure (Fmin) which is having important rule to take a decision for a low noise amplifier, further we will look at other noise parameters optimum reflection coefficient (Gamma opt) and noise resistance (Rn).

According to minimum noise figure point of view ATF 35143 2V, 10m.A., is offering lowest Fmin of 0.12dB compare to all other different process transistors and having Gamma opt value of 0.83 in magnitude and Rn of 0.15.

According to minimum noise figure, optimum reflection coefficient and noise resistance point of view ATF 58143 3V, 30m.A. is offering 0.2dB the second lowest Fmin value compared to ATF 35143 pHEMT and offering lowest values Gamma opt and Rn compared to ATF35143 2V, 10m.A.

Due to the excellent behavior of ATF58143 offering gamma opt is 0.36 in magnitude and noise resistance is 0.04.

So, here interesting point to compare E-pHEMT process based transistors even though having Fmin is a bit larger than pHEMT process and other noise parameters are excellent than pHEMT.

4.3 Comparison of E-pHEMT GaAs process technology based candidates from Avago technology

Here, all the GaAs process technology based transistors has been studied carefully, when looking at the transistors of E-pHEMT technology which is offering low values of optimum reflection coefficient and very low noise resistance compare to all process technologies, drawback is that small amount of increment in minimum noise figure compare to selected pHEMT process as we have discussed earlier in last pages. So, here we are interested to drag all the E-pHEMT technology based transistors together to compare and to have the best transistor noise parameters as a function of frequency and keeping voltage and current as constant.
As we have discussed earlier the processes Si, SiGe, GaAs based transistors. But here just we are interested about GaAs E-pHEMT process based technology transistors. The process candidates are

1) GaAs process technology based transistor ATF-58143 E-pHEMT 3V, 30mA.
2) GaAs process technology based transistor ATF-541M4 E-pHEMT 3V, 40mA
3) GaAs process technology based transistor ATF-54143 E-pHEMT 3V, 40mA,
4) GaAs process technology based transistor ATF 55143 E-pHEMT 2V, 10mA.

4.3.1 Minimum noise figure as a function of frequency

Here the comparisons about the minimum noise figure as a function of frequency, keeping the voltage and current as constant.

The diagram which is showing below comparison of E-pHEMT process technology based transistors noise parameter as a function of frequency.

![Minimum Noise Figure verses Frequency](image)

Figure 4.4: $F_{\text{min}}$ vs Frequency of different process transistors

The above figure 4.4 explains, how the behavior of different E-pHEMT processes.

1) GaAs process technology based transistor ATF-58143 E-pHEMT 3V, 30mA, which is showing lowest minimum noise figure ($F_{\text{min}}$) behavior compared to 3, 4 same process transistors. $F_{\text{min}}$ value is 0.2 dB at 1 GHz frequency and increasing linearly for higher frequencies as a function of frequency

2) GaAs process technology based transistor ATF 541M4 E-pHEMT 3V, 40mA., which is showing lowest minimum noise figure ($F_{\text{min}}$) behavior compared to 1,3,5 E-pHEMT process transistors. $F_{\text{min}}$ value is 0.17 dB at 1GHz frequency and increasing linearly for higher frequencies as a function of frequency.

3) GaAs process technology based transistor ATF 54143 E-pHEMT 3V, 40mA, which is showing lowest minimum noise figure ($F_{\text{min}}$) behavior compared to 4th
process transistor. $F_{\text{min}}$ value is 0.24dB at 1 GHz frequency and increasing linearly for higher frequencies as a function of frequency.

4) GaAs process technology based transistor ATF 55143 E-Phemt 2V, 10m.A, which is showing highest minimum noise figure ($F_{\text{min}}$) behavior compared to above three process transistors. $F_{\text{min}}$ value is 0.27dB at 1GHz frequency and increasing linearly for higher frequencies as a function of frequency.

4.3.2 Conclusion

Compared to all GaAs E-pHEMT process candidates, ATF 541M4 E-pHEMT, which is offering lowest minimum noise figure ($F_{\text{min}}$) value is 0.17dB at 1GHz frequency. Here, these E-pHEMT processes showing minimum noise figure ($F_{\text{min}}$) at narrow band frequency range only and $F_{\text{min}}$ is linearly increasing as a function of frequency. This behavior indicates which is not useful for broad frequency range.

4.3.3 Optimum reflection coefficient ($\Gamma_{\text{opt}}$) as a function of frequency

Here the comparison about the optimum reflection coefficient (magnitude) as a function of frequency, keeping the voltage and current as a constant.

The diagram which is showing below comparison of E-pHEMT process technology based transistors noise parameter as a function of frequency.

![Optimum Reflection Coefficient ($\Gamma_{\text{opt}}$) versus Frequency](image)

*Figure 4.5: $\Gamma_{\text{opt}}$ vs Frequency of different process transistors*

The above figure 4.5 explains how the behavior of different E-pHEMT processes.

1) GaAs process technology based transistor ATF 58143 E-pHEMT 3V, 30m.A, which is showing lowest optimum reflection coefficient ($\Gamma_{\text{opt}}$) behavior compared to 3,4 same process transistors. $\Gamma_{\text{opt}}$ value is 0.36 in magnitude at 1 GHz frequency, decreasing linearly up to the frequencies of 2GHz and increasing linearly for other higher frequencies as a function of frequency.

2) GaAs process technology based transistor ATF 541M4 E-pHEMT 3V, 40m.A, which is showing low optimum reflection coefficient ($\Gamma_{\text{opt}}$) behavior compared
to all 3 same process transistors. Gamma opt value is 0.29 in magnitude at 1 GHz frequency, decreasing linearly up to frequencies of 2GHz and increasing linearly for higher frequencies as a function of frequency.

3) GaAs process technology based transistor ATF 54143 E-pHEMT 3V, 40m.A. which is showing low optimum reflection coefficient (Gamma opt) behavior compared to 1, 4 same process transistors. Gamma opt value is 0.32 in magnitude at 1GHz frequency, decreasing linearly up to frequencies of 2GHz and increasing linearly for other higher frequencies as a function of frequency.

4) GaAs process technology based transistor ATF 55143 E-pHEMT 2V, 10m.A. which is showing high optimum reflection coefficient (Gamma opt) behavior compared to all three same process transistors. Gamma opt value is 0.55 in magnitude at 1GHz frequency, decreasing linearly up to frequencies of 5GHz where Gamma opt is very low and increasing linearly for other higher frequencies as a function of frequency.

4.3.4 Conclusion

Compared to all the behavior of GaAs E-pHEMT process candidates, ATF 551M4 E-pHEMT, which is offering low optimum reflection coefficient (Gamma opt) value is 0.29 in magnitude at 1GHz frequency and also useful for broad band frequency range of our interest.

4.3.5 Noise resistance as a function of frequency:
Here the comparison about the noise resistance (Rn) parameter as a function of frequency, keeping the voltage and current as a constant.

The diagram which is showing below comparison of E-pHEMT process technology based transistors noise parameter as a function of frequency.

![Figure 4.6: Rn vs Frequency of different process transistors](image)

The above figure 4.6 explains the behavior of different E-pHEMT processes.

1) GaAs process technology based transistor ATF 58143 E-pHEMT 3V, 30m.A., which is showing low noise resistance (Rn) behavior compared to all other E-pHEMT
same process transistors. Rn value is 0.04 at 1 GHz frequency and showing flatness up to 2.2GHz frequency and for higher frequencies linearly increasing as a function of frequency.

2) GaAs process technology based transistor ATF 541M4 E-pHEMT 3V, 40m.A., which is showing low noise resistance (Rn) behavior compared to 3rd, 4th E-pHEMT same process transistors. Rn value is 0.05 at 1 GHz frequency and showing flatness for frequencies less than 2.5GHz frequency and for higher frequencies linearly increasing as a function of frequency.

3) GaAs process technology based transistor ATF 54143 E-pHEMT, which is showing low noise resistance (Rn) behavior compared to 2nd, 4th E-pHEMT same process transistors and the same value of 1st process. Rn value is 0.04 at 1 GHz frequency and showing flatness up to 2.2GHz frequencies and for higher frequencies linearly increasing as a function of frequency.

4) GaAs process technology based transistor ATF 55143 E-pHEMT, which is showing high noise resistance (Rn) behavior compared to three above E-pHEMT same process transistors. Rn value is 0.12 at 1GHz frequency, linearly decreasing for higher frequencies up to 5GHz frequency and for higher frequencies Rn value increasing linearly as a function of frequency.

4.3.6 Conclusion

Compared to all GaAs E-pHEMT process candidates, two candidates ATF 58143 E-pHEMT 3V, 30m.A. and ATF 54143 E-pHEMT 3V, 40m.A., are showing flat low noise resistance of 0.04 for a broad frequency range. But here we can choose one of them depending on low cost as per consuming low current is ATF 58143 E-pHEMT.

4.3.7 Overall conclusion for E-pHEMT processes

E-pHEMT processes, here first we will look at one of the noise parameter of transistor is minimum noise figure(Fmin) which is having important rule to take a decision for a low noise amplifier, further we will look other noise parameters optimum reflection coefficient (Gamma opt) and noise resistance (Rn).

According to the minimum noise figure point of view ATF 541M4 3V, 40m.A. is showing lowest Fmin of 0.17dB compare to all other E-pHEMT process transistors and lowest Gamma opt value is 0.29(magnitude compare to all other E-pHEMT process transistors.

According to low noise resistance point of view these both transistors are flat noise resistance and among them ATF 58143 3V, 30m.A. is consuming less current and also offering 0.01 less noise resistance than ATF 541M4 3V, 40m.A.

4.4 Overall conclusion of different process transistors and same E-pHEMT process transistors
According to conclusion of different process transistors, ATF 35143 pHEMT was giving lowest minimum noise figure compare to ATF 581143 E-pHEMT but EpHEMT having lowest gamma opt and Rn values compare to ATF35143. Drawback of ATF 58143 E-pHEMT is taking larger currents.

According to conclusion of E-pHEMT process transistors, ATF 541M4 3V, 40m.A. was giving lowest optimum reflection coefficient and lowest minimum noise figure and noise resistance a bit high compare to ATF 58143 3V, 30m.A. but the drawback of ATF 541M4 E-pHEMT is taking larger currents.

Here over all the conclusion of both process transistors, minimum noise figure point of view ATF 35143 is best option and optimum reflection coefficient point of view ATF 541M4 is best option and noise resistance point of view ATF58143 and ATF 541M4 are can choose but best option is ATF58143 due to consuming less current.

So, further we are interested to look these selected transistors to obtain best candidate for our design goal of low noise amplifier. This goal depends on how designer wants upon choice of noise parameters like minimum noise figure, optimum reflection coefficient, noise resistance. There must be a tradeoff between these parameters to obtain the best candidate. To obtain one of the noise parameter as choice by compromising of other parameters, for our design mainly looking on noise temperature as a function of frequency by changing the value of source impedance for each selected candidate.

4.5 Noise Temperature as a function of frequency by changing the values of Source Antenna Impedance

When the signals are cached by the receiver antenna in a telescope, the impedance of the antennas could be different upon the signal has been cached, behind this antenna low noise amplifier is connected in the chain to amplify the signals to have best signal without noise to get the weakest signal information from the sky.

Now Astronomers want to have best low noise amplifier transistor which will provide lowest noise temperature in the environment of telescope, transistors play a key role to have good noise parameters in making low noise amplifiers to achieve broad band frequency range.

Here, we are interested to look at the broad band frequency range to build a broad band low noise amplifier of our design goal, starting frequency from 500MHz to 1500MHz frequency.

Let us assume the source antenna Impedances starting with minimum noise figure or minimum noise temperature of transistor which is matched to the two port system. So by changing the values of source antenna impedance, realize how would be the noise temperature of the system get affected on broad frequency range of our requirement. From these we can make a conclusion to select a transistor which could provide us having low noise temperature to build a low noise amplifier for the broad band frequency range of our interest.

The diagrams which are showed below the conclusion of E- E-pHEMT processes and different processes of the transistors. Named by ATF-58143 E-pHEMT
candidate, ATF541M4 E-pHEMT candidate and ATF-35143 pHEMT candidate and looking on these selected individual transistor’s noise temperature as a function of frequency by varying antenna source impedance.

4.5.1 ATF-58143 E-pHEMT’s Noise temperature function of frequency

By changing the source antenna impedance of ATF-58143 E-pHEMT 3V, 30m.A. transistor, analyzing the noise temperature as a function of frequency. The resulted plot showed below in the graph and these calculations are made on Matlab.

![ATF-58143 Noisetemp vs Freq](image)

**Figure 4.7: Noise Temp vs Frequency by changing source antenna impedance**

The above figure 4.7 explains the behavior of low noise amplifier’s noise temperature is changing in terms of varied antenna source impedance.

First looking at minimum noise temperature curve which is varying linearly as a function of frequency in the band of our interest. Minimum noise temperature starting from 8K at 500MHz linearly varying and showing the value 31K at 2GHz frequency.

By tanking 50Ohms of antennas source impedance value realized the behavior of noise temperature of the low noise amplifier, the noise temperature starting from 12K at 500MHz linearly varying showing the value 36K at 2GHz frequency.

By applying higher antenna source impedance like 75,100,125,150,200 Ohms, the noise temperature curves varying also linearly as a function of frequency in the band of our interest.

By applying the antennas source impedance less than 25 Ohms, realized the noise temperature behavior in the above diagram is quite interesting. Low noise amplifier’s noise temperature showing 22K which is varied greatly compare to minimum noise temperature of transistor having 8k at same frequency of 500MHz.

4.5.2 ATF-541M4 E-pHEMT’s Noise temperatures as a function of frequency

By changing the source impedance of ATF-541M4 E-pHEMT 3V, 40m.A. transistor, analyzing the noise temperature behavior as a function of frequency.
Figure 4. 8: Noise Temp vs Frequency by changing source antenna impedance

The above figure 4.8 explains low noise amplifier’s noise temperature is changing in terms of varied antenna source impedance.

First looking at minimum noise temperature curve which is varying linearly as a function of frequency band our interest. Minimum noise temperature starting from 6K at 500MHz and linearly varying showing the value 28K at 2GHz frequency. The band from 500MHz to 900MHz range is interesting having flatness even though slightly varying as a function of frequency up to the value of 8K at 900MHz frequency.

By tanking 50Ohms of antenna source impedance value, realized the behavior of noise temperature of the low noise amplifier, the noise temperature starting from 13K at 500MHz linearly varying up to the value of 31K at 2GHz frequency.

By applying higher antenna source impedance like 75,100,125,150,200 Ohms, the noise temperature curves are varying also linearly as a function of frequency in the band of our interest.

By applying the antennas source less than 50Ohms matched system like 25Ohms, the noise temperature behavior is quite interesting. Low noise amplifier’s noise temperature showing 29K at 500MHz and which varied greatly compare to minimum noise temperature of transistor at same frequency.

4.5.3 ATF-35143 pHEMT’s Noise temperature as a function of frequency

By changing the source impedance of ATF-58143 E-pHEMT transistor, analyzing the noise temperature as a function of frequency.
Figure 4.9: Noise Temp vs Frequency by changing source antenna impedance

The above figure 4.9 explains, low noise amplifier’s noise temperature is changing in terms of varied antenna source impedance.

First looking at minimum noise temperature curve which is varying slightly as a function of frequency in the band of our interest. Minimum noise temperature starting from 6 K at 500MHz and linearly varying up to the value of 15K at 2GHz frequency. The band from 500MHz to 900MHz range is interesting, showing flatness even though which is varying slightly as a function of frequency having 8 K value at 900MHz frequency.

By tanking 50Ohms of antenna source impedance value, realized the behavior of noise temperature of the low noise amplifier, the noise temperature starting from 44.95K at 500MHz and linearly varying up to the value of 46.85k at 2GHz frequency.

By applying higher antenna source impedances as like 75, 100, 125, 150, 200 Ohms, the noise temperature curves also varying linearly as a function of frequency in the band of our interest.

By applying the antennas source impedance less than 50Ohms matched system as like 25 Ohms, the noise temperature behavior is quite interesting. Low noise amplifier’s noise temperature showing 88k at 500MHz frequency and which is varied greatly compare to minimum noise temperature of transistor at same frequency.

4.5.4 Overall Conclusion

Compared noise temperature curves as a function of frequency with varying source antenna impedance is giving result to choose one of them as a technological candidate for low noise amplifier design on broad frequency range of our design goal.

ATF-35143 pHEMT is offering lowest minimum noise temperature in the frequency band of our interest starting from 500MHz to 2GHz. pHEMT candidate curves are flat in the entire band of our design goal compare to other two E-pHEMT candidates. Finally we have the best option to take ATF-35143 2V, 10m.A. as a best technological candidate for designing a low noise amplifier for the band of interest and which is also consuming less power compared to E-pHEMTS.
Chapter 5 Fundamentals of Low Noise Amplifier

This chapter gives the basics required for designing low noise amplifiers and the same techniques were adopted during the design process. The most important factors, to be concentrated upon the low noise amplifiers for astronomical purposes are:

- Two port Noise formula
- Noise matching
- Input Matching
- Stability and Gain Considerations

5.1 Two port Noise formula

In this chapter a brief description is given for a noise modeling of two port devices like LNAs. The noise behavior of an LNA or more generally two port network may be described by its parameters, which can be represented in various forms, e.g. using impedances, admittances or reflection coefficients. The four noise parameters and the properties of the source connected to the two port input fully determine the effective noise temperature of the two ports. The formula in noise temperature,

\[
T_N = T_{\text{min}} + \frac{4R_n T_0}{Z_0} \left( \frac{\Gamma_s - \Gamma_{\text{opt}}}{1 + \Gamma_{\text{opt}}} \right)^2 \left( 1 - \left| \Gamma_s \right|^2 \right)
\]

With \( T_0 = 290 \text{K}, Z_0 \) the normalized impedance, \( \Gamma_s \) the source reflection coefficient

\( T_{\text{min}}, R_n, \Gamma_{\text{opt}} \) are the four noise parameters of two port.

From 5.1 it is obvious that \( T_N = T_{\text{min}} \) for \( \Gamma_s = \Gamma_{\text{opt}} \) (noise matching) [18].

The noise temperature formula can also be written as Noise figure

5.1.1 The Noise Temperature as a Function of \( \Gamma_s \)

The noise figure of a linear two-port amplifier can be formulated as a function of only four parameters:

1) \( T_{\text{min}} \), the minimum noise temperature of the device/transistor
2) \( \Gamma_{\text{opt}} \), the optimum source reflection coefficient for achieving \( T_{\text{min}} \)
3) $R_n$, the device noise resistance

4) $\Gamma_s$, the actual source reflection coefficient applied to the input of the device

Three of the four parameters in Equation 5.1 are fixed constants that are determined by the device characteristics at a given frequency. It is interesting to note that, apart from the device constants that cannot be changed; the noise figure for the amplifier is completely determined by the source impedance $Z_s$ or source reflection coefficient $\Gamma_s$.

Since the noise temperature is a function of only one variable, $\Gamma_s$ is the value in this case, only that gives the desired noise figure. Only one value of $\Gamma_s$ ($\Gamma_s = \Gamma_{opt}$) gives the minimum noise temperature. Other values of $\Gamma_s$ yield larger noise temperatures and the solution set for any noise temperature larger than $T_{min}$ is represented by a circle(called a noise circle) on the Smith chart.

Just considering to bring $\Gamma_s$ value to $\Gamma_{opt}$ of transistor, means to match the $\Gamma_s = \Gamma_{opt}$ to get minimum noise temperature at a single frequency called as noise matching topology, some noise matching topologies will be discussed in following section.

### 5.2 Noise matching topologies

As from [18] briefly can describe $\Gamma_s = \Gamma_{opt}$ is called as noise matching at single frequency. Matching the $\Gamma_s$ value till reaching the load, i.e. $\Gamma_{opt}$ at input terminal.

Some matching topologies should be adopted to bring the $\Gamma_s$ to the point $\Gamma_{opt}$ is described to have a noise matching for two port network of LNA.

At higher frequencies, matching is usually done by micro strip lines. Less than 2GHz range of frequencies like for astronomical purposes used L-section matching networks.

#### 5.2.1 L-Section matching networks

L-Section utilizes purely reactive components such that no power is dissipated in the matching networks. Smith chart is an extremely useful tool to design L-section matching networks [19].

From the Appendix figure 1.1 two of them are chosen for our designing purposes. L-section design is best performed on an Admittance/Impedance or Impedance Admittance smith chart (ZY Smith Chart).

L-section design match can be obtained by a single Impedance chart or Admittance chart, which would be easy but a bit time consuming. Admittance and Impedance chart which is a bit confusing but easy to match the topology while working on two charts at same time.
Adding series reactive loads will modify the impedance by adding negative reactance (series C), or positive reactance (series L).

Adding shunt reactive loads will modify the admittance by adding negative susceptance (shunt C), or positive susceptance (shunt L).

The Admittance/Impedance chart is shown below with the curves of reactance and susceptance. The Smith chart provides visual insight into the feasibility of design. The effective of adding series and shunt elements in the ZY Smith chart is attached in the Appendix 1.2.

5.2.2 Series Inductance with shunt capacitance noise matching topology

In this topology, looking from the load side towards source side for noise matching, load is here as $Z_{opt}$. The diagram is shown below. $jx$ as series inductance and $jb$ as shunt capacitance.

![Diagram](image)

*Figure 5.1: Series reactive with shunt susceptive L section matching [20]*

As shown in the above figure 5.3 which is related to working in impedance and admittance smith chart (ZY Smith Chart) adding $jx$ (series inductance) in impedance chart which move us to the point where conductance circle is intersecting. At this point by adding $jb$ (shunt susceptance) on admittance chart reach us to the point which is our goal of optimum impedance. The source impedance has matched to the optimum impedance of the system.

The matching circuit which is parallel obtained as series inductance with Shunt Capacitance.

The formulas which are shown below it's easy to calculate the reactive and susceptive values at a single frequency [21]

For a series C component:

$$C = \frac{1}{\omega XN}$$  \hspace{1cm} (5.2)

For a series L component:

$$L = \frac{XN}{\omega}$$  \hspace{1cm} (5.3)

For a shunt C component:

$$C = \frac{B}{\omega N}$$  \hspace{1cm} (5.4)

For a shunt L component:
\[ L = N/\omega B \]  \hspace{1cm} (5.5)

The mathematical calculations are written down in the Simulation chapter and smith chart is attached in the Appendix 1.3.

5.2.3 Series Capacitance with Shunt Inductance noise matching topology

In this topology, looking from the load side towards source side for noise matching as like in 1\textsuperscript{st} noise matching, load is here as \( Z_{opt} \). The diagram is shown below. \( jx \) as series capacitance and \( jb \) as shunt inductance.

![Figure 5.2: Series reactive with shunt susceptive L section matching [20]](image)

As shown in the above figure 5.4 which is related to working in impedance and admittance smith chart (ZY Smith Chart) adding \( jx \) (series capacitance) in impedance chart which move us to the point where conductance circle is intersecting. At this point by adding \( jb \) on admittance chart reach us to the point which is our goal of optimum impedance. The source impedance has matched to the optimum impedance of the system.

The mathematical calculations are written down in the Simulation and smith chart is attached in the Appendix 1.4.

5.2.4 Small piece of transmission line with Quarter wave transformer noise matching topology

The quarter wave transformer is useful and practical circuit to match a real load impedance to a transmission line. If only a narrow band matching required, a single section transformer is sufficient. For broad band matching, multi-section transformer may be designed.

One drawback of the transformer is it can only match real impedance. At first, complex load impedance always be transformed to a real impedance, however by using a length of transmission line between the load and the transformer or an appropriate series or shunt reactive stub. These techniques usually alter the frequency dependence of the equivalent load, which often has the effect of the reducing the bandwidth of the match [22]

A single section transformer wave matching transformer circuit is shown in fig5.5 characteristic impedance of the matching section is

\[ Z_v(\frac{\lambda_0}{4}) = \sqrt{Z_s Z_L} \]  \hspace{1cm} (5.6)
Where \( Z_s = \text{Source impedance} \)
\( Z_L = \text{load impedance} \)

![Figure 5.3: Quarter wave transformer matching [22]](image)

At the desired frequency \( f_0 \), the electrical length of the matching section is \( \lambda_0/4 \), but at other frequencies the length is different, so perfect match is no longer obtained. When we use transmission line we can move towards generator only to reach the object not like as lumped elements. By using lumped elements can move in the whole smith chart in either way.

**The topology when \( Z_s \) and \( Z_L \) are real**

The diagram is shown below. The topology when both \( Z_s = R_s \) and \( Z_L = R_L \) are purely real and since we need \( Z_{in} = R_s \), we can use the equation for impedance on a \( \lambda_0/4 \) line.

Which is \( Z_{in} = Z_0^2/Z_L \)

Thus, if we set \( R_s = Z_0^2/R_L \) we can solve \( Z_0 = \sqrt{R_s R_L} \).

Thus choosing \( \lambda_0/4 \) with this characteristic line will provide the desired match.

![Figure 5.4: Quarter wave transformer matching real load to real source impedance[23]](image)

**Quarter wave transformer: Complex \( Z_L \) and real \( Z_s \)**

The diagram is shown below. Here the topology when \( Z_L \) is complex and \( Z_s \) is real.

In this case, we use an extra length of line \( l \) to convert \( Z_L \) in to a purely real impedance \( Z_B \). Then we match \( Z_B \) to \( Z_s \) using the above discussed topology when both source and load impedances are real.

Since \( Z_{in} = Z_0^2/Z_B \), we find \( Z_0 = \sqrt{R_s Z_B} \).
We find $Z_B$ and $l$ using the smith chart. Plot $Z_L/Z_0$ on the chart and then rotate clockwise until the real axis is reached where $Z_{in}$ is purely real.

Read off the value there and un normalize to find $Z_B$. The distance rotated to get the real axis is $l$. [23]

![Figure 5.5: Quarter wave transformer matching complex load to real source impedance [23]](image)

If the load impedance point is having positive imaginary value, for noise matching this positive imaginary value of load should take as negative imaginary value for noise matching. This way is opposite to the power matching [24]

In other way to explain the diagram in words, by staying at source side looking towards the load side.

The mathematical calculations are written down in the Simulation and smith chart is attached in the Appendix 1.5.

5.2.5 Long piece of transmission line with the quarter wave transformer noise matching topology

The same procedure here as already was discussed in the 3rd noise matching topology. But here using a long piece of transmission line instead of using a short piece of transmission line as used in 3rd noise matching topology.

5.2.6 Quarter wave length transmission line with long piece of transmission line noise matching topology

The quarter wave transformer theory was explained in the 3rd noise matching topology. The 3rd noise matching topology as shown in figure, which is travelling from load impedance (optimum impedance) towards source impedance. The way in 3rd noise matching topology for noise matching load impedance imaginary part was negative.

But here in this case of 4th noise matching, which is opposite way to the noise matching was explained in the 3rd noise matching topology. The load impedance also positive imaginary part as the transistor’s load impedance (optimum impedance) is located.

The way of noise matching, moving from source to the load as we did in 1st and 2nd noise matching topologies.
5.2.7 Quarter wave transformer with the small piece of transmission line noise matching topology

This procedure of noise matching topology was discussed in the 5th noise matching topology.

The mathematical calculations are written down in the Simulation and smith chart is attached in the Appendix 1.5.

5.2.8 Quarter wave length transmission line with the shunt inductance:

The theory of quarter wave transformer as already discussed in the 3rd noise matching topology just here discussing briefly.

Here this noise matching topology is also opposite to the power matching in a sense that load imaginary part value will become negative for this matching.

In this topology starting from the load moving towards source, first one is by using shunt inductance in impedance and admittance smith chart (ZY Smith chart), which made load impedance to reach the real axis on the smith chart from the negative value of the smith chart. Second is by using quarter wave length from the real axis could reach to the centre of the smith chart where the source impedance is located.

As this method is convenient to move on the smith chart while using lumped elements. As we have noticed the complex load impedance easily reached to the real axis by using lumped elements not like transmission lines which should move only on generator side or in forward direction.

The mathematical calculations are written down in the Simulation and smith chart is attached in the Appendix 1.6.

5.2.9 Conclusion

These seven noise matching topologies which were discussed above could be used on ADS to see the results. As it shows the results working at single frequency only for noise matching. But we are interested to look the noise matching issue for broad band frequency range. To obtain broad band frequency for designing low noise amplifier, we may have to loose noise matching at single frequency and this may lead to get broad band frequency with some mismatch.

Firstly, noise matching is the main issue in designing low noise amplifier, Secondly, to obtain power matching and noise matching simultaneously at broad band frequency range, there must be tradeoff to have better noise match or power match.

Further we will continue below with Input matching.
5.3 Input Matching

To deliver the maximum power from the antenna to the LNA, matching to the impedance of antenna, e.g., 50Ω, is required at the input port of the LNA. For wideband applications, this impedance matching should be obtained over a wide frequency range at the input port of the LNA and is usually a major challenge considering the noise and power consumption requirements [25]:

Where the condition for input match, \( Z_s = Z_{in}^* \) or \( Z_{in} = Z_s^* \)

In this expression \( Z_s \) is the source impedance.

\( Z_{in} \) is the input impedance looking in to the transistor.

\( Z_{in}^* \) is the impedance looking from source towards transistor's input impedance, this impedance, is imaginary, is opposite to the impedance \( Z_{in} \), but the real impedance is the same for both.

\( Z_s^* \) is the impedance looking from transistor's input side (\( Z_{in} \)) towards source impedance(\( Z_s \)). The imaginary part of \( Z_s^* \) is opposite to the imaginary part of \( Z_s \) but the real impedance is same for both.

Further is the discussion, how to reach the input match for wide band applications. So, its necessary to discuss the several architectures which offer input match of 50 Ohms to LNA.

There exist several architectures that generate the required 50Ω impedance at the input port of the LNA. The diagrams are shown below which offer wide band input match and the brief description will be in continuation.

![Figure 5.6: Different input matching topologies (a) resistive termination (b) \( 1/g_m \) termination (c) shunt feedback (d) inductive degeneration [6]](image-url)
Some popular topologies are as shown in Fig. 5.8. The simplest method to obtain matching over a wide range of frequencies is to use the resistive termination illustrated in Fig. 5.8 (a). However, this method affects from a relatively high NF due to the thermal noise of resistive termination.

An alternative approach to achieve input matching is to use the source of a pHEMT device as the input termination, symbolically depicted in Fig. 5.8 (b). In common-gate architecture, the impedance looking into the source terminal of active device is $1/gm$. Therefore, proper bias and sizing of the LNA will result in $1/gm=50$ and satisfies the matching requirement. However, there still exists the problem of high NF with this architecture.

Shunt feedback amplifier suggests yet another solution for achieving the required matching at the input port (see Fig. 5.8 (c)). This type of amplifier employs negative feedback to generate the $50\Omega$ impedance at the input port. This architecture still suffers from the thermal noise of the shunt resistor; however, the lower bound on NF is usually smaller than that of resistive and $1/gm$ terminations.

To overcome the deteriorous effect of real resistors on the NF of LNAs, designers suggest the use of inductively degenerated LNA to generate the required input impedance.

Further we are going to discuss in detail about the inductively degenerated LNA.

### 5.4 Inductively degenerated LNA

In 1928 H. Nyquist showed that the noise from any impedance is determined by its resistive component [26]. Consequently, if an ideal lossless element is used to provide the feedback then the minimum noise measure is unaffected [26].

The below diagrams are showed. Fig 5.9 is FET symbol, Fig 5.10 is FET symbol while added ideal inductor in series with the source.

![Figure5. 7: FET Symbol left and Simplified FET model right [26]](image)

![Figure5. 8: FET Model with External source inductance [26]](image)
The additional inductance between the source and ground provides lossless negative series feedback to accomplish the following results.

The voltage developed across the internal $C_{gs}$ capacitor is $V_c = I_g \frac{1}{(SC_{gs})}$ where $S = \sigma + jw$.

$$Z_{in} = \frac{V_g}{I_g} = \left( I_g R_g + V_c + I_S S L_s \right) / I_g$$  \hspace{1cm} (5.7)

Substituting $I_g \frac{1}{(SC_{gs})}$ for $V_c$ and $(I_g + g_m V_c)$ for $I_S$ gives:

$$Z_{in} = \frac{V_g}{I_g} = \left( I_g R_g + I_g \frac{1}{(SC_{gs})} + S(I_g + g_m V_c) L_s \right) / I_g$$  \hspace{1cm} (5.8)

Again, substituting $I_g \frac{1}{(SC_{gs})}$ for $V_c$ and dividing through by $I_g$ gives:

$$Z_{in} = \frac{V_g}{I_g} = \left( I_g R_g + I_g \frac{1}{(SC_{gs})} + S(I_g + g_m I_g / SC_{gs}) L_s \right) / I_g$$  \hspace{1cm} (5.9)

Rearranging and canceling out $I_g$ in the last term yields the result:

$$Z_{in} = \left( R_g + g_m L_s / C_{gs} \right) + S(L_s + 1 / S^2 C_{gs}) L_s$$  \hspace{1cm} (5.10)

Substituting $S = jw$ into the above gives the input impedance as a function of frequency:

$$Z_{in} = R_g + g_m L_s / C_{gs} + j[wL_s - 1/(wC_{gs})]$$  \hspace{1cm} (5.11)

Equation 5.11 is the new composite FET input impedance and this equation can be rewritten for clarity as follows:

$$Z_{in} = R_g + R_a + j[X_{ls} - X_{e_{gs}}]$$  \hspace{1cm} (5.12)

where $[R_a = g_m L_s / C_{gs}]$ is effectively an “added” input resistance.

The input impedance of the FET without feedback can be written down by inspection (from Figure 5.9) as

$$Z_{in} = R_g - jX_{e_{gs}}$$  \hspace{1cm} (5.13)

Thus, equation 5.11 indicates that feedback adds $R_a + jX_{ls}$ to the FET’s input impedance.

From the above result, it is clear that a real (resistive) component equal to $g_m L_s / C_{gs}$ has been added to the input impedance as well as a positive reactive component.

Both of these effects move $Z_{in}$ closer to $Z_{opt}^*$. It can be shown that for the frequency and amount of feedback applied here that $Z_{opt}$ does not change appreciably. Low noise GaAs FETs, stating that “$Z_{opt}$ remains relatively unchanged with the addition of source inductance”[27]. Thus, as $Z_{in}$ moves closer to $Z_{opt}^*$ the distance between the noise match and the gain match on the Smith Chart decreases, facilitating a simultaneous gain and noise match.

Since the feedback is negative, there is an accompanying decrease in gain with increasing feedback. Therefore, a compromise is generally made between the
amount of improvement in input, output reflection coefficient, noise figure and the
gain reduction one is willing to take.

To summarize, the important requirements of an LNA are low NF, good input
matching. With these goals in mind, we will now start our study of the to obtain goal
to design low noise amplifier for broad band range of application in the area of
astronomical purposes.

5.5 Wide band noise and Input matching

Input matching was obtained while adding source inductive feedback to match input
LNA. Obtaining power matching and noise matching at frequency of 0.5 to 1.5GHz,
there should be compromise in terms of minimum noise figure for noise matching
and input reflection coefficient for power matching.

To obtain the wideband noise and input matching, the source impedance seen from
the gate of the input transistor ($Z_S$ shown in pozar2334) should be the complex
conjugate of the input impedance, $Z_{in}$ (to deliver the maximum power) and at the
same time be equal to $Z_{opt}$ (to achieve $\text{NF}_{\text{min}}$). Thus the following four conditions
should hold over the entire frequency band of interest:

\[
\begin{align*}
\text{Real}\{Z_{opt}\} &= \text{Real}\{Z_S\} \\
\text{Imag}\{Z_{opt}\} &= \text{Imag}\{Z_S\} \\
\text{Real}\{Z_{in}\} &= \text{Real}\{Z_S\} \\
\text{Imag}\{Z_{in}\} &= \text{Imag}\{-Z_S\}
\end{align*}
\]

Combining the above criteria, simultaneous noise and input matching are achieved
when:

\[Z_{in} = Z_{opt}^* \quad \text{or} \quad Z_S = Z_{opt} = Z_{in}^* \quad (5.14)\]

In this above expression $Z_{opt}$ is the transistor’s optimum impedance.
$Z_{opt}^*$ is optimum impedance looking from the source side towards the transistor’s
optimum impedance $Z_{opt}$ while having imaginary part opposite to the $Z_{opt}$ and both
are having same real impedance

To satisfy this equation we should analyze the real and imaginary parts of the two
impedances $Z_{in}$ and $Z_{opt}$.

Before starting the design of low noise amplifier there is a necessary to discuss
about the stability and gain considerations.

5.6 Stability and gain considerations
The stability of an amplifier is a very important consideration in a design and can be determined from the S-Parameters. Starting with s-parameters are in brief has explained to understand about the concept of stability.

5.6.1 S Parameters
Two-port networks are described in numerous ways. The most well-known description is to relate the four variables of input/output voltage/current by using a 2×2 matrix. Depending on which two of these four elements are selected as the independent variables, different matrices can be defined. Impedance (Z) matrix, admittance (Y) matrix, and hybrid (H) matrix are the most common matrices that define the two-port network voltage-current relation. In order to find the elements of these matrices, certain short and open-circuit tests must be performed on the network. However, these tests might not be possible at very high frequencies where open and short tests fail due to the existence of stray capacitances and inductances as well as transmission line effects.

![Figure 5.9: S parameters definition of two-port networks](image)

The inability to perform short and open tests and the possibility of harming the circuit during these tests suggest the use of an alternative solution to characterize the network at high frequencies [28]. One popular solution is the introduction of the Scattering parameters (simply S parameters), which defines the four variables as the incident/reflected input/output voltage waves (or powers).

The definition of S parameters exploits the fact that a transmission line terminated in its characteristic impedance does not reflect any power at its termination [29]. To show the usefulness of this property, consider the block diagram of a two-port network shown Fig. 2.9 where $Z_0$ is the impedance of the source and the load terminations and $E_{ii}$ and $E_{ri}$ are the magnitude of incident and reflected voltage waves, respectively. The S parameter coefficients are expressed as:

$$b_1 = s_{11}a_1 + s_{12}a_2$$

$$b_2 = s_{21}a_1 + s_{22}a_2$$

Where

$$a_1 = E_{ii}/\sqrt{Z_0}$$

$$a_2 = E_{i2}/\sqrt{Z_0}$$

$$b_1 = E_{r1}/\sqrt{Z_0}$$

$$b_2 = E_{r2}/\sqrt{Z_0}$$

The normalization to the square root of $Z_0$ makes the square of magnitude of $ai$ and $bi$ equal to the incident and reflected power at both ports.
Now, if we terminate port two in $Z_0$, which sets $a_2$ equal to zero, and apply a power source to port one, we obtain the following relations:

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} = \frac{E_{r1}}{E_{i1}}$$

$$S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} = \frac{E_{r2}}{E_{i1}}$$

Where $S_{11}$ is called the input reflection coefficient and is a practical measure for the impedance matching at the input port of the LNA and $S_{21}$ represents the forward gain of the amplifier.

If, on the other hand, port 1 is terminated to $Z_0$ and power is sent from port 2:

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} = \frac{E_{r1}}{E_{i2}}$$

$$S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} = \frac{E_{r2}}{E_{i2}}$$

Where $S_{11}$ is the reverse transmission or gain of the network and $S_{22}$ is called the output reflection coefficient of the network.

Using these definitions, we can predict that a good amplifier should possess a large $S_{21}$ to achieve high gain, small $S_{11}$ and $S_{22}$ to possess good input and output matching, and very small $S_{12}$ to ensure stability and reverse isolation. The typical values of S parameters for an LNA are $S_{11}$ and $S_{22}$ <-10dB, $S_{21}$ >10dB, and $S_{12}$ <-40dB, which may vary according to the application.

### 5.6.2 Stability consideration

The stability of an amplifier is a very important factor; the stability condition of a network is frequency dependent, so that it is possible for an amplifier to be stable at its design frequency but unstable at other frequencies.

In the figure5.12, oscillations are possible if either the input or output port impedance has a negative real part: which means $\Gamma_{in} > 1$ or $\Gamma_{out} > 1$, Where $\Gamma_{in}$ and $\Gamma_{out}$ are the reflection coefficients seen looking at the input and output of the terminated network. In terms of S-parameters they are defined as;
\[
\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_{L}}{1 - S_{22}\Gamma_{S}}
\]

(5.17)

\[
\Gamma_{out} = S_{22} + \frac{S_{12}S_{21}\Gamma_{S}}{1 - S_{11}\Gamma_{L}}
\]

(5.18)

Again \(\Gamma_{S}\) and \(\Gamma_{L}\) are called as reflection coefficient seen looking toward source and load respectively and in terms of S-parameters it can be defined as;

\[
\Gamma_{S} = \frac{Z_{S} - Z_{0}}{Z_{S} - Z_{0}}
\]

(5.19)

\[
\Gamma_{L} = \frac{Z_{L} - Z_{0}}{Z_{L} - Z_{0}}
\]

(5.20)

Where \(Z\) term represents the impedances of source, load and characteristic impedances respectively. As because \(\Gamma_{in}\) and \(\Gamma_{out}\) depends on source and load matching networks, the stability of the amplifier depends on \(\Gamma_{S}\) and \(\Gamma_{L}\) as presented by matching networks.

The stability check can be done using Rollets stability factors \(K\) and \(\Delta\), Where \(K\) and \(\Delta\) in terms of S-Parameters are as follows;

\[
K = \frac{1 - S_{11}^{2} - S_{22}^{2} + \Delta^{2}}{2|S_{12}S_{21}|} > 1
\]

(5.21)

\[
\Delta = S_{11}S_{22} - S_{12}S_{21} < 1
\]

(5.22)

Here we define two types of conditions for stability check:

- Unconditionally Stable
- Conditionally Stable

**Unconditionally Stable:**
The network is said to be unconditionally stable when \(K > 1\) and \(\Delta < 1\) for all Passive source and load impedances.

**Conditionally Stable:**
This condition is also called as potentially unstable, this is the case when \(K < 1\) and \(\Delta < 1\) for a certain range of passive source and load impedances. for a certain range of passive source and load impedances i.e. \(\Gamma_{in} < 1\) or \(\Gamma_{out} < 1\).

From the practical point of view, most microwave transistors produced by the manufacturers are either Unconditionally stable or potentially unstable. In fact, in potentially unstable transistors most practical values of \(K\) are such that \(0 < K < 1\). These potentially unstable transistors have source and load stability circles that intersect the boundary of the smith chart. Usually at low frequencies the transistors are unstable as we can see from the output plot of the designed amplifier.
Stability check:
The stability conditions can be known by plotting smith chart for both Source and Load sides respectively. The circle centre and radius can be calculated and the same can be plotted for both Source and Load to check out the stable and unstable regions with respective S-Parameters. This stability circles not only decides the stability of the transistor but also help much in developing Input and Output matching circuits in turn enhances the design of LNA. Referring the above figure;

Towards Source

\[ C_s = \frac{\left(S_{11} - \Delta S_{22}^*\right)}{|S_{11}|^2 - |\Delta|^2} \]  \hspace{1cm} (5.23)

\[ R_s = \frac{|S_{12}S_{21}|}{|S_{11}|^2 - |\Delta|^2} \]  \hspace{1cm} (5.24)

![Figure 5.11: (a) Smith chart showing stable and unstable regions in \( \Gamma_L \) plane (b). Smith Chart showing stable and unstable regions in \( \Gamma_s \) plane [9]](image)

Towards Load

\[ C_L = \frac{\left(S_{22} - \Delta S_{11}^*\right)}{|S_{22}|^2 - |\Delta|^2} \]  \hspace{1cm} (5.25)

\[ R_L = \frac{|S_{12}S_{21}|}{|S_{22}|^2 - |\Delta|^2} \]  \hspace{1cm} (5.26)

Using the above equations and introducing the given S-Parameters of the transistors one can check it out the Input and Output Stability Circles.
Unilateral and Bilateral cases:

With respect to the S-Parameter from the available transistor, there is a possibility to define two cases while designing LNA. When $S_{12} \neq 0$ the case is said to be Bilateral otherwise Unilateral i.e. $S_{12} = 0$. Mostly Bilateral case is used by the manufacturers in the designs.

Unilateral Case:

In many practical cases $|S_{12}|$ is small enough to be ignored, and the device can then be assumed to be unilateral which greatly simplifies the design procedure.

The error in the transducer gain caused by approximating $|S_{12}|$ to zero and is given by

$$\frac{1}{(1+U)^2} < \frac{G_T}{G_{TU}} < \frac{1}{(1-U)^2}$$

(5.27)

Where $U$ is defined as the Unilateral Figure of merit and mathematically is

$$U = \frac{|S_{12}S_{21}S_{13}S_{22}|}{1-|S_{11}|^2 |1-|S_{22}|^2|}$$

(5.28)

Bilateral Case:

When the case is said to be Bilateral, then the input and output sections should match simultaneously, i.e. $\Gamma_S = \Gamma_{opt}^*$ and $\Gamma_L = \Gamma_{out}^*$. Where,

$$\Gamma_{out}^* = S_{22} + \frac{S_{21}S_{12} \Gamma_{opt}}{1-S_{22} \Gamma_S}$$

(5.29)

$$\Gamma_{in}^* = S_{11} + \frac{S_{21}S_{12} \Gamma_L}{1-S_{22} \Gamma_L}$$

(5.30)

5.6.3 Gain Considerations

Besides Stability, the LNA has to provide adequate gain as well. We can thus define separate elective gain factors for the Input matching network(Source), the transistor itself, and the Output matching network(Load) and hence are as follows:

Figure 5. 12: General transistor amplifier circuit
Then the overall transducer gain is

\[ G_T = G_S G_0 G_L \]  \hspace{1cm} (5.34)

The effective gains from \( G_S \) and \( G_L \) are due to the impedance matching of the transistor to the impedance \( Z_0 \).

### 5.6.4 Stability Technique

To keep the stability factor in the unconditionally stable region, the stabilization method must be applied in the system. The most simple and effective way to stabilize an active device is to add a series resistance or a shunt conductance to the port. However adding a series resistance to a port may add too much noise into the system noise characteristic because the series resistance, which is adding the noise source, is placed in the signal path.

Therefore it is recommended to add shunt conductance to the port. In this case, the conductance should be small enough to avoid signal flow. In other words, a large enough shunt resistance should be added to the port.

Further next chapter will start with procedure and results.
Chapter 6 Simulations

6.1 Design of a single ended Low Noise Amplifier

In the previous chapter we have seen many different possibilities for the input and noise matching topology of the LNA. Now to link the theoretical aspect with the experimental one, some simple simulations will be shown. As discuss earlier the technology used for this design is ATF35143-pHEMT transistor which has down loaded from Avago technologies, the biasing points are at 2V, 10m.A. the simulation software used is ADS version 2005A from Agilent.

Requirement:

The aim of this study is to provide the best performance as possible with a given technology, to achieve it, it’s necessary to take into account all the requirements:

- Noise: figure: less than 0.5 dB (35K),
- Gain : between 20 to 30 dB,
- Slope Gain: 3dB in all the band,
- Frequency range: [0.5-1.5] GHz,
- Input reflection (S11): as low as possible
- Output reflection (S22): as less than as possible
- Unconditional stable

It is fundamental to know the most important constraint in designing LNAs is noise figure in over all band of frequency and some compromises also come in picture while depending on gain, input and output reflection coefficient.

Further this chapter has been extended with noise matching topologies at narrow band frequency, broad band frequency range and input matching topology for power matching on broad band frequency range and both selected topologies are conjugated to obtain broad band input noise matching topology for low noise amplifier for astronomical purposes.

6.1.1 Design a single ended LNA matched with two ports

The LNA which just having transistor with matched to 50 ohms ports and the figure is showed below. First, looking at the LNA’s noise figure which should be obtain to minimum noise figure $F_{\min}$
The result obtained from Figure 6.1 is showed below with badly matching to 50Ohms ports.

From the above Figure 6.2, realized that the noise figure ($nf(2)$) is very high as varying from 0.626 to 0.642dB with in the frequency band of 0.5 to 1.5GHz while $NF_{\text{min}}$ is varying from 0.1 to 0.17dB on the broad band of same frequency range.

To match this LNA to obtain minimum noise figure, different topologies were discussed as in the theory to obtain LNA noise figure equal to minimum noise figure, now it will be added with the practical work to choose a best topology.

6.1.2 Noise matching topologies while applying on badly matched LNA

In this section noise matching topologies has explained with mathematical solution and the figure to achieve the minimum noise figure means Optimum reflection coefficient have to match the Source reflection coefficient of the two port network at single frequency of 1GHz and at broad frequency range of 0.5 to 1.5GHz.
6.1.3 Series inductance with shunt capacitance noise matching topology

As already discussed in theory about this noise matching topology, here the below section is about the mathematical solution and the results from ADS.

Mathematical solution:

The chosen transistor ATF-35143pHEMT having the normalized value of Zopt=3.36+j4.95(r+jx) at the single frequency of 1GHz.

Zopt value is in impedence, either we can change to Yopt as well. Starting with Impedance and admittance smith chart (Z/Y smith Chart), Zopt is which is quite far from center of the smith chart or near about to the border of the smith chart. Zs which is 50Ohms at the centre of the smith chart. To obtain minimum noise figure at singe frequency Zs should be rotate in smith chart that should be transferred to Zopt. Where Zs=Zopt value could brought us minimum noise figure.

Zs value is 1Ohm(normalized to 50Ohms) which is at centre of the smith chart. From this point taking larger part of series inductance(j3.01) on r=1 circle bring us to the point where the constant conductance circle also intersects the r=1 circle, from this point by adding shunt capacitance(-j0.13) brought us to the point where Zopt is located(3.36+j4.95).

The matching circuit which is parallel obtained as series inductance with Shunt Capacitance.

The formulas which are discussed in the theory, it's easy to calculate the reactive and susceptive values at a single frequency.

After the calculations from those formulas

Series L=23.95nH

Shunt C=0.5168pF

The worked smith chart for this topology is attached in the Appendix 1.3. In this design at input side, input matching circuit was obtained from the above mentioned values. The circuit designed on ADS showed in the below diagram using with the large series inductance (Series L=23.95nH) at the gate terminal which is behind to the 50Ohms port and the small amount of shunt capacitance (Shunt C=0.5168pF) in parallel to the gate terminal which is behind to the transistor’s input side.
Figure 6.4: Result of series inductance with shunt capacitance noise matching topology

The above resulted figure 6.5 has shown that has matched at 1GHz frequency, Minimum Noise figure (NFmin) of transistor is equal to the noise figure (nf(2)) at port 1 and at the wide range of frequency from 500 MHz to 1.5 GHz., the curve is varying like a slope from 500MHz to 1GHz and the slope has taken the shape of linearity from 1GHz to 1.5GHz, means at lower frequencies and higher frequencies noise is linearly varying.

6.1.4 Series Capacitive with shunt inductive noise matching topology

As already discussed the theory about this noise matching topology, here the below section is about the mathematical solution and the results from ADS.

Mathematical Solution:

As already discussed the Z_{opt} value in the 1\textsuperscript{st} noise matching topology. To obtain Z_s=Z_{opt}. The calculation is showed below

Z_s value is 1Ohm (normalized to 50Ohms) which is at centre of the smith chart. From this point by adding larger part of series Capacitance (-j3.01) on r=1 circle and at the same time constant conductance circle also intersects the r=1 circle, from this
point by adding shunt inductance (j0.2998) brought us to the point where Zopt is located (3.36+j4.95).

The matching circuit which is parallel obtained as series capacitance with Shunt inductance.

After the calculations from formulas

Series C=1.0575pF
Shunt L=18.302nH

The worked smith chart for this topology is attached in the appendix. In this design at input side, input matching circuit was obtained from the above mentioned values. The design on ADS showed in the below diagram using with the small amount of capacitor in series (Series C=1.0575pF) to the gate terminal which is behind to the 50Ohms terminal and large part of inductor (Shunt L=18.302nH) in parallel to the gate terminal which is behind to the transistor’s input side.

Figure 6.5: Series Capacitive with shunt inductive noise matching topology

The figure 6.7 is obtained is the matched with this topology and the resulted figure is showed below at wider frequency range.

Figure 6.6: Result of Series Capacitive with shunt inductive noise matching topology
In the above figure 6.8 minimum noise figure (NFmin) is matched to the noise figure \(nf(2)\) on port1 at single frequency of 1GHz. The curve which is in the plot varies like a slope from 500 MHz to the 1GHz range. At 500 MHz noise figure is too high compare to the 1 GHz frequency and when it reaches to the 1.5GHz frequency again noise figure increased like 0.523dB value which is more than minimum noise figure.

6.1.5 Quarter wave transformer with a small piece of transmission line noise matching Topology

As already discussed in theory about this noise matching topology, here the below section is to see the mathematical solution.

Mathematical solution:

In 3\(^{rd}\) noise matching topology we travelled from normalized \(Z_{\text{OPT}}=(3.36-j4.95)\) to normalized \(Z_S=1\ \Omega\) means towards the centre of the smith chart. But here in this case of 4\(^{th}\) noise matching, moving from normalized \(Z_S=1\ \Omega\) towards normalized \(Z_{\text{OPT}}=(3.36+j4.95)\) where this is located, this \(Z_{\text{OPT}}=(3.36+j4.95)\) value which is located at the same place where the actual transistor’s noise parameter \(Z_{\text{OPT}}=(3.36+j4.95)\) is located in the smith chart.

Here the way of noise matching, moving from source to the load as we did in 1\(^{st}\) and 2\(^{nd}\) noise matching topologies. The \(Z_{\text{OPT}}=(3.36+j4.95)\) value is located at the same point on the smith chart which was discussed in 1\(^{st}\) and 2\(^{nd}\) noise matching topologies as the transistor’s \(Z_{\text{OPT}}\) noise parameter location of ATF-35143 pHEMT.

The normalized \(Z_{\text{OPT}}\) value of ATF-35143 pHEMT is 3.36+j4.95, which lies on the Impedance smith chart having imaginary value positive.

For this noise matching, starting from centre of the smith chart where \(Z_S=1\ \Omega\) (normalized) to reach \(Z_{\text{OPT}}\) (normalized) complex value on the smith chart, this way also opposite way to the power matching [18] for this procedure.

In other sense by staying at load side looking towards the source side.

Source side, \(Z_S=1\ \Omega\) (normalized) which is located at the centre of the impedance smith chart on the real axis. Starting from source side by using quarter wave length transmission line take us to the point where \(Z_{S1}\) is located having the real value 0.09, from \(Z_{S1}\) point by using half wave length transmission line reach us to the complex load impedance \(Z_{\text{OPT}}=(3.36+j4.95)\), \(Z_{\text{OPT}}\) where it is located in wave length having 0.2278 \(\lambda\).

At start by adding quarter wave transformer take us to the \(Z_{S1}\) is located.

Un normalized value of \(Z_{S1}=(0.09)(50)=4.6049\ \text{Ohms}\).

\[
Z_{\frac{1}{4}} = \sqrt{Z_{S1}Z_S} = \sqrt{(4.6049)(50)} = 15.1738\ \Omega
\]
From $Z_{S1}$ point, travelled wave length transmission line is $0.2278\, \lambda$. At this point real value becomes complex value by using half wave length transmission line.

Re normalizing the $Z_{S1}$ value with the characteristic impedance of the quarter wave length transmission line $Z_{\frac{\lambda}{4}}$,

$$Z_{S1}/Z_{\frac{\lambda}{4}} = 4.6049/15.1738 = 0.3036.$$ 

This value where the voltage is minimum on the impedance smith chart. From this point by drawing quarter wave length transmission line on the impedance smith chart take us to the point where voltage has maximum at 3.29 on the right hand side of smith chart.

If we multiply voltage maximum value with quarter wave length transmission line $Z_{\frac{\lambda}{4}}$ then multiplied result should be normalized to reach the $Z_S$ at centre of the smith chart having the normalized value of $1\, \Omega$.

$$V_{\text{max}} \cdot Z_{\frac{\lambda}{4}} = (3.295)(15.174) = 49.99\, \Omega,$$

this value get normalized with $50\, \Omega$ to have the value of $Z_S = 1\, \Omega$ which is normalized.

The worked smith chart is attached in the appendix. In this design to match at input side, input matching circuit was obtained from the above mentioned values. The design on ADS showed in the below diagram using the quarter wave transformer with the small piece of transmission line.

![Figure 6.7: Quarter wave transformer with a small piece of transmission line noise matching Topology](image)

The simulated plot of this figure 6.10 has showed in the below diagram.
The above figure 6.11 shows, minimum noise figure (NFmin) of the transistor has matched to the noise figure (nf(2)) on the input side at single frequency of 1Ghz frequency and at the wide frequency from 500 MHz to 1.5GHz., the plot seems to be like oscillating, which is quite different from the above two topologies at wide frequency. The noise figure nf(2) 2.431 dB is quite high at 500 MHz and noise figure 0.12 dB is matched at 1 GHz and noise figure 2.502dB is quite high at 1.5 GHz. Means at lower frequencies and higher frequencies noise is high compared to 1GHz single frequency matched system.

The figure which is like oscillating noise figure, the nature of this transmission line for our design showing higher noise figure at wide frequency range. Further other noise matching topologies are also tested to look what could be the result, from the above diagram and from other resulted transmission line matching topologies are oscillating at wide frequency range. The conclusion could be drawn these noise matching topologies will not be useful for our design goal of low noise amplifier for astronomical purposes.

6.1.6 Quarter wave transformer with shunt Inductance noise matching topology

The normalized $Z_{opt}$ value of ATF-35143 pHEMT is 3.36+j4.95, which lies on the Impedance smith chart with imaginary value as positive

Mathematical solution:
As explained above for noise matching $Z_{opt}$=3.36-j4.959 (normalized) is having negative imaginary value. $Z_{opt}$ Which is having complex load has used shunt inductance to reach the real axis of the smith chart. The method of using lumped elements to match either load side or source side was discussed in the 1st and 2nd noise matching topology.

The calculated shunt inductance value is $L=58.94 \text{ nH}$ from the formulas in 1st noise matching topology.
By using shunt inductance the complex load \( Z_{\text{req}} \) which is reached to the real axis having the real impedance value 10.895\( \Omega \) (normalized).

From this real impedance \( Z_{10.895\Omega} \), by using quarter wave transformer will take us to the centre of the smith chart where \( Z_S = 1\Omega \). This real load to real source impedance method was discussed in the 3rd noise matching topology.

Travelled quarter wave length transmission line is \( 0.25\lambda \).

Renormalized value of \( Z_{10.895\Omega} = (10.895)(50) = 543.975\Omega \)

At this point by adding quarter wave transformer take us to the centre of the smith chart where \( Z_S \) is located.

\[
Z_{\lambda/4} = \sqrt{Z_{10.895\Omega} Z_S} = \sqrt{(543.975)(50)} = 164.92\Omega
\]

Re-normalizing the \( Z_{10.895\Omega} \) value with the characteristic impedance of the quarter wave length transmission line \( Z_{\lambda/4} \).

\[
Z_{10.895\Omega} / Z_{\lambda/4} = 543.975 / 164.92 = 3.29
\]

This value where the voltage is maximum on the impedance smith chart. From this point by drawing quarter wave length transmission line on the impedance smith chart take us to the point where voltage has minimum at 0.3036 on the right hand side of smith chart.

If we multiply voltage minimum value with quarter wave length transmission line \( Z_{\lambda/4} \), then multiplied result should be normalized to reach the \( Z_S \) at centre of the smith chart having the normalized value of 1\( \Omega \).

\[
V_{\min} Z_{\lambda/4} = (3.295)(15.174) = 49.99\Omega
\]

This value get normalized with 50\( \Omega \) to have the value of \( Z_S = 1\Omega \) with is normalized.

The worked smith chart is attached in the appendix. The matching circuit which has designed using quarter wave transformer and the susceptive inductance. The circuit is showed in the diagram.
Figure 6.9: Quarter wave transformer with shunt Inductance noise matching topology

The simulated plot of the matching circuit showed in the below diagram.

Figure 6.10: Results of Quarter wave transformer with shunt Inductance noise matching topology

In the above diagram this topology matched at 1GHz frequency having a noise figure of 0.12dB and at wide frequency, on 500 MHz noise figure nf(2) is 0.909dB is higher than the minimum noise figure and at 1 GHz is matched to the minimum noise figure of single frequency and at 1.5 GHz noise figure nf(2) is 0.699dB is higher than the required minimum noise figure.

This noise matching topology has been matched to the narrow band frequency range and for wide band frequency range is showing higher noise figure.

6.1.7 Conclusion

The above showed four noise matching topologies which are giving minimum noise figure only at the single frequency 1 GHz and it differs at the point while looking for the wide frequency range between 500 MHz to 1.5 GHz. These four plots are at wide frequency range is offering the information which could be suitable to take for our design.

In four of the noise matching topologies, one of them could be avoided which is used transmission lines obtained the results with the oscillating nature of the noise figure on wide frequency range and the rest of the three topologies could be look for tuning on wide frequency operation to obtain flat wide band minimum noise figure to design low noise amplifier.
6.2 Tuning or Optimization of selected three topologies

From the conclusion, we know that three noise matching topologies are obtained the noise figure is also high except at 1GHz frequency range. But here we will tune three selected topologies to obtain minimum noise figure over wide frequency range of our interest.

6.2.1 Series inductance with shunt capacitance tuned noise matching topology

The tuned result is showed below in the diagram.

![Diagram of Series inductance with shunt capacitance tuned noise matching topology](image1)

Figure 6.11: Results of Series inductance with shunt capacitance tuned noise matching topology

The above figure 6.15 is showing for wider frequency range, the noise figure got worse but showed flat noise figure over broad band of our interest.

6.2.2 Series Capacitive with shunt inductive tuned noise matching topology

The below diagram showed after tuning the circuit.

![Diagram of Series Capacitive with shunt inductive tuned noise matching topology](image2)

Figure 6.12: Results of Series Capacitive with shunt inductive tuned noise matching topology

The above figure 6.16 is showing for wider frequency range, the noise figure got worse but it showed flat noise figure over broad band of our interest.
6.2.3 Quarter wave transformer with shunt Inductance tuned noise matching topology

This topology has tuned over broad frequency range and the resulted graph is showed below.

![Figure 6.13: Results of Quarter wave transformer with shunt Inductance tuned noise matching topology](image)

The above figure 6.17 showing worse noise figure than minimum noise figure of transistor and moreover this noise figure is quite good than above tuned two topologies.

6.2.4 Conclusion

From the above three tuned topologies using quarter wave length with shunt inductance topology id offering good noise figure compare to other two topologies. These topologies were studied during optimization. Further some components are added to chosen topologies at input side of LNA to look the impedance at every added component to obtain minimum noise figure over wide band frequency of our interest.

Here, the reason to choose Series inductance with shunt capacitive topology is by nature pHEMT transistor has the capacitance between gate and source pins. So, we chose this topology for having inductance in series to obtain minimum noise figure.

The quarter wave transformer used topology is also chosen due to the results were obtained minimum noise figure over wide frequency range of our interest. So, further discussion starts with adding components to selected topologies.

6.3 Adding components to tuned series inductance with shunt capacitance for noise matching

As already discussed about this noise matched circuit at single frequency and was tuned for wide frequency range of our design requirement. The circuit which was tuned and the given response was bad noise figure at broad frequency range. So, there is requirement to add components to match this circuit at the input side for noise matching and we will look other parameters as well gain and input and output
reflection coefficients. The final circuit is added by components has showed below in the diagram.

We saw the results while the circuit with out adding the components was showing flat noise figure was already explained and the same circuit has tuned for minimum noise figure and has been showed flat noise figure having the values like at 0.5GHz, 1GHz, 1.5GHz are 0.518 dB, 0.236dB, 0.287dB and the resulted graph is varying like a slope, here only these values are mentioned from the ADS and the plot is not included.

Adding inductance in parallel to the tuned circuit has showed the noise figure which was get close to minimum noise figure only at 1 GHz like 0.190 dB, at rest frequencies goes down to bad compare to the above results like 0.619, 0.337.

By adding capacitance in series the noise figure has improved at 500MHz, 1GHz,1.5GHz are 0.323dB,0.231dB,0.289dB. This result is improved at 0.5GHz, 1.5GHz but at 1GHz again noise figure is get worst than minimum noise figure.

By adding capacitance in parallel the result has improved at all frequencies and the final circuit of this added components has showed in the below diagram. This is showing flat noise figure comparing to all results which were discussed in the above lines by adding one by one component.

![Figure6. 14: Adding components to tuned series inductance with shunt capacitance for noise matching](image)

The figure 6.18 simulation’s noise figure plot 1.7 is attached in the appendix. Appendix 1.7 is showing the minimum noise figure at all frequencies in the band from 500MHz, 1GHz, 1.5GHz like 0.298dB, 0.260dB, 0.260dB.

In terms of noise temperature the graph is showed in the below diagram
Figure 6.15: Noise Temperature of adding components to tuned series inductance with shunt capacitance for noise matching

In the above figure 6.20, the noise temperature is varying in the band from 20K to 17K which is quite reasonable values.

The below diagram is showing the gain which is varying over wide frequency range.

Figure 6.16: Gain of adding components to tuned series inductance with shunt capacitance for noise matching

The above figure 6.21 is showing the 5dB decay in the gain from 500MHz to 1.5GHz frequency range.

Resulted Input and output reflection coefficients are showed in the below diagram.
6.4 Adding components to quarter wave transformer with shunt Inductance noise matching topology

This circuit was explained already for tuning. Here some components are added to obtain the minimum noise figure for broad band of our interest. As already has showed the noise figure after tuning the circuit at frequencies like 500 MHz, 1GHz, and 1.5GHz are 0.408dB, 0.202dB, 0.193dB and also we are interested to look other parameters gain and input and output reflection coefficients.

First by adding series capacitance the noise figure become more better like at the frequencies of 500MHz,1GHz,1.5GHz are 0.259dB,0.202dB,0.193dB.

By adding one more series capacitance at input side the result was showing good noise figure at 500MHz frequency and at other frequencies a bit has increased. The final response after adding components has showed below in the diagram.
Figure 6.18: Adding components to quarter wave transformer with shunt Inductance noise matching topology

The resulted output from figure 6.23 is showed in the appendix 1.8 in terms of noise figure and is showing the curves which behaves like a ripple noise figure. The results at frequencies band of 500MHz, 1GHz and 1.5GHz are 0.110dB, 0.249dB, 0.274dB. The resulted noise figure is acceptable but showing ripple could lead us to not to have flat noise figure.

The below diagram is showed in terms of noise temperature.

Figure 6.19: Noise temperature of adding components to quarter wave transformer with shunt Inductance noise matching topology

In the above figure 6.25 the temperature is varying like a ripple from 7K to 18K in the band from 0.5GHz to 1.5GHz frequency.

The below diagram which is showing the gain across the band.
Figure 6.20: Gain of adding components to quarter wave transformer with shunt Inductance noise matching topology

The above figure 6.26 is showed the gain is varying from 23dB to 13dB on frequency range of 0.5 to 1.5GHz and the decay of 10dB in the gain.

The below diagram which is sowed for input and output reflection coefficient.

Figure 6.21: Reflection Coefficients of adding components to quarter wave transformer with shunt Inductance noise matching topology

From the above figure 6.27, realized that the input reflection coefficient is bad over frequency range of 0.5 to 1.5 GHz having less than zero value and except at 1GHz frequency which is less than one. Output reflection coefficient is less than one varying from -8dB to -16dB in frequency band of our interest and at lower frequencies less than 500MHz greater than one.

6.5 Conclusion

The first selected topology by adding components to tuned series inductance with shunt capacitance noise matching is showing the good results compare to quarter
wave transformer topology. While obtained noise figure is low, gain is good with less decay.

Quarter wave transformer with shunt inductance showing good noise figure and good gain but showing ripple in the band of our interest which could not be suitable for our design goal. Output reflection coefficient $S_{22}$ is greater than 1 at 450MHz which can do bad matching at output.

These two topologies are at single frequency and wide frequency

1) Noise figure which is showing good in over all band even though worse than minimum noise figure of transistor.
2) $S_{11}$ is less than -1 at single frequency but at wide frequencies which is less than 0.
3) Gain is good at single frequency, for wide range frequencies gain roll off 5dB in first topology and 10dB gain roll off in second topology.

Noise figure could be acceptable but the $S_{11}$ and gain are not reliable and acceptable over wide frequency range.

To improve the input reflection coefficient ($S_{11}$), we can add source inductance $L_s$ at source terminal.

To improve the $S_{22}$ we have to match the output side as like input match.

Further to improve the power matching at input side, a real inductor is introduced at source lead and input matching topology is analyzed by the ADS in the below pages.

### 6.6 Effect of source Inductance for Input matching

The below diagram which is badly matched LNA to the 50Ohms input and output ports without using matching circuit. As we have seen already during in the last pages for noise figure which was showing overall 0.6dB noise figure. Here in this below diagram we are looking in terms of input impedance $Z_{in}$ for impedance matching and Optimum impedance $Z_{opt}$ for noise matching.

The figure 1.8 with out source feed back inductance is attached in the appendix and that shows real part of input impedance $Z_{in}$ is 12Ohms at 1GHz frequency and real part of optimum impedance $Z_{opt}$ is 166Ohms at 1GHz frequency. From this we know that input impedance is quite smaller than optimum impedance.

So, first to improve the input impedance of real part to the real value of optimum impedance while using source inductance as a feedback at source terminal is as shown in below figure.

Source feed back Inductance Mathematical Solution:
\[ R_s = 168\Omega \ (R_{opt}), \text{ (from the data sheet)} \]

\[ C_{gs} = 0.15 \text{ pF} \ (\text{from the data sheet}) \]

\[ g_m = 0.09 \text{ mho} \ (\text{from the data sheet}) \]

\[ R_s = g_m L_s / C_{gs} \quad (\text{formula}) \]

\[ L_s = 2.8 \text{ nH} \]

This source inductance \( L_s \) value is implemented in the below diagram.

---

**Figure 6.22:** a) The above figure adding source inductance at source terminal will give real impedance at gate terminal. b) Source Inductance for Input matching

From the resulted figure 6.29, some mismatch was occurred. So, the source inductance was tuned to obtain the real input impedance is equal to optimum real impedance and the result of the tuned effect of source inductance showed in below figure.

---

**Figure 6.23:** Effect of source Inductance for Input matching

The above figure 6.30 is resulted while added source inductance. The input impedance of real \( Z_{in} \) and the optimum impedance of real \( Z_{opt} \) are matched on 169.585Ohms at single frequency.
By adding source inductance which took us from 12 ohms value of $\text{real}(Z_{in})$ to 169.585 which is showing that power matching and noise matching obtained at 1GHz single frequency. Means added source inductor given us feedback real impedance with positive imaginary part at input side of the transistor as showed in the diagram and the imaginary part of $Z_{in}$ looking from source side is 176 Ohms while imaginary part of optimum impedance is 229Ohms at single frequency. Small amount of Imaginary part also improved while adding source inductance.

### 6.7 Conclusion

Added source inductance for good power matching to achieve input impedance equal to optimum impedance and realized that it works only at narrow band frequency range while matched real part and imaginary part remains to match.

From this input matching ideas are come up to obtain noise matching and power matching simultaneously over wide frequency of our interest. Here from these resulted figures on broad band frequency range, matching could be added to match imaginary part and to obtain power matching and noise matching at overall band frequency range from 0.5 to 1.5GHz. Further discussion is to obtain noise matching and power matching simultaneously over broad frequency range of our design goal.

### 6.8 Wide band noise and Input matching

In this section, noise matching is merged with added source inductive feedback LNA to obtain wide band noise and input matching LNA. Obtaining power matching and noise matching at frequency of 0.5 to 1.5GHz frequency of our interest is challenging work. Tradeoff should be considered in terms of minimum noise figure for noise matching and input reflection coefficient for power matching and obtaining both matching for wide frequency range could be difficult.

As already explained the criteria in theoretical part to obtain minimum noise figure and input matching simultaneously.

Thus the following four conditions should hold over the entire frequency band of interest:

\[
\begin{align*}
\text{Real}(Z_{opt}) &= \text{Real}(Z_S) \\
\text{Imag}(Z_{opt}) &= \text{Imag}(Z_S) \\
\text{Real}(Z_{in}) &= \text{Real}(Z_S) \\
\text{Imag}(Z_{in}) &= \text{Imag}(-Z_S)
\end{align*}
\]

Combining the above criteria, simultaneous noise and input matching are achieved when:

\[Z_{in} = Z_{opt}^* \quad \text{or} \quad Z_S = Z_{opt} = Z_{in}^*\]

To satisfy this equation we should analyze the real and imaginary parts of the two Impedances $Z_{in}$ and $Z_{opt}$. 76
In this matching series capacitive with shunt inductance while adding source inductance feedback is used.

Added source inductance with just two ports matching could give the value of positive real impedance and positive imaginary impedance at input side as explained in theoretical aspect. To compensate this added positive imaginary value, input matching selected as a series capacitance with parallel inductance at input side of the transistor.

And for power matching the imaginary part is having positive impedance cause of added source inductance while using series inductance with shunt capacitance noise matching topology having positive imaginary value and which could not brought us for good power matching, it could bring us noise matching.

So, here, Series capacitive with shunt inductance noise matching while adding source inductive feedback topology is used and as showed in below diagram.

Figure 6.24: Wide band noise and Input matching

The resulted output from figure 6.31 is showed in the below diagram.

Figure 6.25: Results of Wide band noise and Input matching

From the resulted fig 6.32, \( \text{Real}\{Z_{opt}\} = \text{Real}\{Z_s\} = 101.779 \)
\[
\text{Imag}\{Z_{\text{opt}} l\} = \text{Imag}\{Z_s\} = -159.146 \\
\text{Real}\{Z_{\text{in}} l\} = \text{Real}\{Z_s\} = 122.65 \\
\text{Imag}\{Z_{\text{in}} l\} = \text{Imag}\{-Z_s\} = -130.542
\]

From the above compared values are proven there is mismatch to obtain minimum noise figure and power match as well. The diagram which is showed below in terms of noise temperature.

Figure 6.26: Noise temperature of Wide band noise and Input matching

The resulted figure 6.33 is quite reasonable for noise temperature in the band of our interest even though which is not flat across the band.

The factors noise temperature which is quite reasonable. So, we are now interested to look at the stability of LNA. Stability should be stable at higher frequencies and at lower frequencies due to the source antenna impedance of the LNA would be changed and the system should be stable for our require band and out of band as well.

The below diagram which is showing for stability, normally at low frequencies the transistor showed instability. The stability of below diagram showed after applied wide band matching.

Figure 6.27: Stability of Wide band noise and Input matching

In the above figure 6.34, stability has improved compare to with out wide band noise matching and stability is less than one in the band of our interest but it should have
grater than 1. If we could not get the stability in band and out band frequency regions the system would cause oscillation even we have obtain good noise figure and input matching.

Here important to get stability at desired frequency range of 0.5 to 1.5GHz, at lower frequencies less than 500MHz and higher frequencies above 1.5GHz as well. So, system should perform stability greater than one cause the LNA which is dependent on antenna source impedance.

**6.9 Stability**

Stability should be greater than one in the band and out of band as well. As given adding small resistance in series to the gate and greater amount of resistance at drain to stabilize the circuit [19].

Series resistance may cause noise figure due to the lossy element nature of the resistance. We can apply shunt resistance at gate side to stabilize the circuit.

From the last plot of stability, stability is less than one at lower frequencies and higher frequencies as well. To obtain stability grater than one at lower frequencies series LR filter added as parallel to the gate.

The below diagram shows after applying LR circuit parallel to the gate and to obtain stability greater than one at in band of our frequency range from 0.5 to 1.5 GHz.

![Figure 6.28: Adding Shunt LR filter to wide band noise and input matching](image)

The resulted output from figure 6.35 is showed below.
From the above figure by applying LR filter in parallel to the gate side. Mismatch has occurred on optimum impedance for noise matching and input impedance for power matching at single frequency.

By applying LR filter at input side of the transistor, real optimum impedance get affected which is less than the real value of transistor’s optimum impedance but the real input impedance which is greater than the real optimum impedance. There is a mismatch occurred between two impedances.

The stability plots can analyze from the below diagram.

The above figure 6.37 is showing by applying shunt LR filter to the gate and that was given the stability greater than one at desired frequency of 0.5 to 1.5GHz and also at less than 500 MHz frequency but at higher frequencies causing instability.

The below diagram is showing behavior of noise temperature.
The above figure 6.38 is explaining while added shunt LR filter added noise figure in to the LNA. There is trade off to have stability over noise figure and input matching.

6.10 Conclusion

The single ended low noise amplifier was designed with different noise matching topologies to obtain noise match, added source inductive feed back to obtain input impedance matching and noise matching at single frequency. Here was the challenging work to obtain simultaneously noise match and power match over broad range frequency of our interest. This was the goal of design.

Further wide band noise and input matching topology was implemented to obtain broad band frequency range of our interest and this topology was given the interesting noise temperature in the band of our interest but the drawback was stability less than one in the band of our interest so we introduced LR filter.

There should be a tradeoff to obtain NF and input put matching and stability. Using the LR filter, stability was improved which is greater than one at lower frequencies and also in the band of our interest but NF and input match get worsted and the Stability also less than one at higher frequencies.

Due to these draw backs of single ended LNA, so we are now interested to look on two stage amplifier to have good noise matching and power matching at input side. Good gain and output matching at output side but the stability should be greater than one in band and out band of frequencies. Stability also could be solved by two stage amplifier.

Further the two stage LNA design is continued with brief theory and this would be the solution to obtain stability, NF, $S_{11}$, $S_{22}$ and gain parameters.
6.11 Design of two stage Low Noise Amplifier

Two stage amplifier designed for low noise figure and maximum flat gain and good input and output reflection coefficient.

At Lower frequencies two stage amplifier was designed, given low noise temperature. The amplifier is designed with inductive feedback with simple two stages [30]. The second stage was employed to provide a high gain [31].

As explained in the single ended low noise amplifier about the specific goal of LNA. The two stage LNA consisting of two transistors; First stage single ended amplifier drain is added with gate terminal of second stage transistor. Here the second stage transistor model is also same as the first transistor model and having same specifications.

First stage is mainly designed for low noise and input matching. Second stage is added due to improve mainly for output matching, gain and improvement in stability purposes as well.

Drain of first stage will not be needed to add components due to the second stage of LNA. Usually in single ended LNA first stage output side is matched to get good output matching but we are designing two stages. In two stage LNA by adding components to drain of first stage will add noise which could decrease noise degradation. To avoid that, components are added at drain side of second stage for output matching.

The below diagram which is analyzed for stability purposes looking on two stage amplifier. First stage transistor is added by a source inductive feedback and the second transistor source is grounded.

![Figure 6.32: Cascade Low Noise Amplifier](image)

The simulated figure 6.39 for stability is shown below in the diagram.
The above figure 6.40 shows, by adding second stage the stability is greater than one but the compared stability values are double in numbers with the values of designed first stage amplifier from 0.5 to 1.5GHz frequency of our interest. At other frequencies showing instability.

The second plot is showed below for noise and power match.

![Figure 6.33: Stability of Cascade Low Noise Amplifier](image1)

The output is written down from the above figure 6.41.

\[
\begin{align*}
\text{Real}\{Z_{\text{opt}1}\} &= \text{Real}\{Z_S\} = 174.648 \\
\text{Imag}\{Z_{\text{opt}1}\} &= \text{Imag}\{Z_S\} = 215.882 \\
\text{Real}\{Z_{\text{in}1}\} &= \text{Real}\{Z_S\} = 172.491 \\
\text{Imag}\{Z_{\text{in}1}\} &= \text{Imag}\{-Z_S\} = -13.736
\end{align*}
\]

From the above compared values are proven there is mismatch to obtain a noise figure but which is very low. Power match is certainly mismatched of larger difference, there is necessary of matching at input side for noise and power match. The resulted noise temperature output is shown below in the diagram.

![Figure 6.34: Results of Cascade Low Noise Amplifier](image2)
The resulted noise temperature from the above figure 6.42 which is somewhat acceptable even this noise temperature is higher than minimum noise temperature.

The result for the gain can be seen from below diagram.

The above figure 6.43 is showing larger decay in the gain between the frequencies of our design goal. The starting frequency 500 MHz having the value of 16dB gain and at 1.5GHz frequency showing the value of 8dB which means 8dB decay in the frequency band of our interest.

The resulted input reflection coefficient and output reflection coefficient showed in below diagram.

Figure6. 36: Gain of Cascade Low Noise Amplifier

Figure6. 37: Reflection coefficients of Cascade Low Noise Amplifier
From the above diagram $S_{11}<1$ at frequencies of our design interest and at high frequencies $S_{11}>1$. $S_{22}<1$ at frequencies of design interest and at higher frequencies $S_{22}>1$.

The $S_{11}$ and $S_{22}$ are showing greater than 1 at higher frequencies means high reflections are obtaining which cause the larger power mismatch at higher frequencies.

Further we are interested to extending design to obtain optimum wide band noise matching and input matching.

### 6.12 Wide band noise and input matching with two stages

Here the first stage is similar as used already in the design of single ended Low noise amplifier, the second stage is added with source grounded transistor. The new two stage design is showed in the below diagram.

![Diagram](image)

**Figure 6.38:** Wide band noise and input matching with two stages

The resulted stability diagram is showed below.

![Stability Diagram](image)

**Figure 6.39:** Stability of Wide band noise and input matching with two stages
From the above figure 6.46, the stability is increased at less than 500MHz frequency and also in the band of our interest.

The resulted optimum impedance and input impedance graph showed below in the diagram.

Figure 6.40: Results of Wide band noise and input matching with two stages

The output is written down from the above figure 6.47.

\[
\text{Real}\{Z_{\text{opt}}\} = \text{Real}\{Z_S\} = 87.8 \\
\text{Imag}\{Z_{\text{opt}}\} = \text{Imag}\{Z_S\} = -6.614 \\
\text{Real}\{Z_{\text{in}}\} = \text{Real}\{-Z_S\} = 62.765 \\
\text{Imag}\{Z_{\text{in}}\} = \text{Imag}\{-Z_S\} = -40.38
\]

From the above compared values are proven there is mismatch to obtain a noise figure but which is very low. Power match is certainly mismatched of greater difference. So, there is necessary of matching at input side for noise match and power matching as well.

The resulted below diagram according to noise temperature

Figure 6.41: Noise temperature of Wide band noise and input matching with two stages
In the above Figure 6.48 noise temperature has increased in the required band varying from 62K to 43K, the noise temperature has been increased to unacceptable value and which should be minimized to obtain minimum noise temperature.

The resulted gain can be seen from the below diagram

![Diagram](image)

**Figure 6.42: Gain of Wide band noise and input matching with two stages**

From the above figure 6.49 the gain is showing 38dB at starting frequency of 500MHz and 24dB at 1.5GHz frequency. The decay of gain in the band like as 14dB. This decay in gain is not acceptable for our design. The gain should be flat with high required gain.

The result of the $S_{11}$ and $S_{22}$ can be seen from below diagram

![Diagram](image)

**Figure 6.43: Reflection coefficients of Wide band noise and input matching with two stages**

In the above figure 6.40 $S_{11}$ is increased to -24dB at starting frequency of 500MHz which is quite good result and further $S_{11}$ is decreasing up to -4dB at frequency of 1.5GHz in the band of our interest.

And $S_{22}$ is increased to -6dB at starting frequency of 500MHz and $S_{22}$ is varying as a function of frequency up to -11dB at frequency of 1.5GHz in the band of our interest.
6.13 Conclusion

Using two stage amplifier, as first stage amplifier with source inductive feedback and second stage with source as grounded. Stability problem was solved up to some extent at some frequencies and noise figure is also obtained to minimum noise figure without matching. The gain is improved compare to single ended amplifier in the band of our interest. Input reflection coefficient less than one at required band of our interest.

Further we extended design to obtain optimum wide band noise matching and input matching. The stability is increased using wide band matched circuit having shunt LR filter at the input gate side of the first stage LNA. The noise temperature has increased in the required band. The good gain is obtained with decay in the band of our design goal. $S_{11}$ is improved and $S_{22}$ also improved in the band of our interest.
Chapter 7 Discussion and Conclusion

First the single ended low noise amplifier was designed with different noise matching topologies to obtain noise match, added source inductive feed back to obtain input impedance matching and noise matching at single frequency. Here was the challenging work to obtain simultaneously noise match and power match over broad range frequency of our interest. This was the goal of design.

Further wide band noise matching topology was implemented to obtain broad band frequency range of our interest and which was interesting noise temperature in band of our interest. But the drawback was stability less than one in band frequency of our interest so we added shunt LR filter.

There was a tradeoff to obtain NF and input put matching and stability. Using shunt LR filter, stability was greater than one at lower frequencies and also at the band of interest but NF was worse and input match worse as well. Stability also was less than one at higher frequencies.

Before finishing the summary of single ended LNA it would be better to introduce some circuits which were tried on ADS using single ended LNA. Two more circuits were designed using single ended LNA.

One circuit was made with T-net work consisting of inductances in series with capacitance in parallel at input side and output side matched to a series high resistor value with inductance in parallel. Response was obtained 0.4dB over all noise figure and stability greater than one in band and at higher frequencies except at lower frequencies. $S_{11}$ and $S_{22}$ less than one and gain was larger decay in the required band. Due to high resistance at output will influence noise figure at input side of the transistor for astronomical aspects this circuit was avoided.

Other circuit was made on ADS with extended components(series capacitance with shunt inductance) with T-net work consisting of inductance in series with capacitance in parallel at input side and used RC feedback network through output to input side for stability purposes, $S_{11}$ and $S_{22}$ also was improved but the noise figure was get worse.

Due to these draw backs of single ended LNA, two stage amplifier was designed, first stage amplifier with source inductive feedback and second stage with source as grounded.

Using two stage amplifier, stability problems were solved at some frequencies and noise figure is also obtained to minimum noise figure without matching, the gain is improved, input and output reflection coefficient less than one at required band of our interest.

Further we extended the design to obtain optimum wide band noise matching and input matching. The stability was increased using wide band matched circuit having shunt LR filter at the input gate side of the first stage LNA. The noise temperature
has increased in the required band. The good gain is obtained with decay in the band of our design goal. $S_{11}$ was improved and $S_{22}$ was also improved in the band of our interest.

### 7.1 Future work

This thesis work could be extended with two stage amplifier for astronomical purposes.

Input matching and noise matching should be improved at input side.

Stability should be greater than one over all frequency of 0 to 20GHz frequency.

Output matching should be obtained with specified gain and output reflection coefficient.

Biasing and Layout.
Appendix

1.1) Single frequency matching networks

![Diagram of single frequency matching networks.](image1)

Figure 1.1: Diagram of single frequency matching networks.

1.2) Effect of adding series and shunt elements in the ZY Smith chart

![Effect of adding series and shunt elements in the ZY Smith chart.](image2)

Figure 1.2: Effect of adding series and shunt elements in the ZY Smith chart
1.3) Smith chart solution for Series inductance with shunt capacitance noise matching topology

Figure 1.3: Smith chart solution for series inductance with shunt capacitance
1.4) Smith chart Solution for series capacitive with shunt inductive noise matching topology

Figure 1.4: Smith chart solution for series capacitive with shunt inductive noise matching topology
1.5) Smith chart solution for Quarter wave transformer with a small piece of transmission line noise matching Topology

Figure 1.5: Smith chart solution for Quarter wave transformer with a small piece of transmission line noise matching Topology
1.6) Smith chart solution for Quarter wave transformer with shunt Inductance noise matching topology

Figure 1.6: Smith chart solution for Quarter wave transformer with shunt Inductance noise matching topology
1.7) Noise figure of adding components to tuned series inductance with shunt capacitance for noise matching

![Figure 1.7: Noise figure of adding components to tuned series inductance with shunt capacitance for noise matching](image)

1.8) Noise Figure of adding components to quarter wave transformer with shunt Inductance noise matching topology

![Figure 1.8: Noise Figure of adding components to quarter wave transformer with shunt Inductance noise matching topology](image)

1.9) Without effect of source Inductance for Input matching

![Figure 1.9: Without effect of source Inductance for Input matching](image)
References


