DESIGN AND PROTOTYPING OF A LOW-SIDE ACTIVE CLAMP FORWARD CONVERTER POWER SUPPLY

Comparison with an existing Fixed Frequency Resonant Power Supply

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Preface

Many thanks to John, PSU Engineering and PSG for sharing and support.
Abstract

This thesis details the design, build and commissioning of an active clamp forward converter with synchronous rectification and comparison to an existing fixed frequency resonant switching converter power supply. The points of comparison are: noise and ripple, power efficiency, number of components, size of components and cost. The goal is to increase the efficiency by 10% and reduce the cost and component count by 33% as compared to the existing design. A partial implementation of the new design was completed in the project timeframe and a provisional comparison showed a promising efficiency and reduced component count for comparable cost. Design improvements are proposed and follow up work is discussed to prototype a complete unit and confirm these results.
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1 Introduction

Switch mode power supplies are a major component in modern electronic equipment and must often be designed to meet conflicting criteria, requiring compromises to be made in the design. Therefore engineers are continuously investigating new topologies of switch mode power supplies that enable them to be designed with fewer compromises between the design criteria, while still producing power supplies that are robust and more efficient. One such topology is the active clamp forward converter with synchronous rectification. Provided that the theory is sound this topology should provide increased efficiency with a decrease in the number of components required compared to existing fixed frequency converters. The attraction with the active clamp forward converter is that it implements zero voltage switching on the primary side, the same as the existing power supply but with synchronous rectification on the secondary side. The synchronous rectification helps to minimize the conduction losses in the power supply. A choice of a low side switching configuration was made due to the high voltages involved and a floating high side switching MOSFET was considered unwise. The difficulty with the low side active clamp approach in this case is the high voltage aspect, as the existing power supply’s boost voltage is 320 VDC and this will have a negative impact on the size of all components, especially the semiconductors on the primary side.
2 Theory

2.1 Power Supply Basics

A power supply is basically a converter and all converters are based on the idea of having an input power, converting this in some way and getting an output power. There is a multitude of different types of converters: DC-DC converters, AC-AC cycloconverters, DC-AC inverters but the subject of this thesis is a variety of the AC-DC converter, that is, taking a voltage of a sinusoidal waveform at a certain frequency as input and getting a DC voltage as output.

Within the AC-DC converter family there are two major types of power supply technologies: linear regulators and pulse width modulated switching power supplies, the latter more commonly named switch mode power supplies. Within this group of power supplies there is again a multitude of different ways to accomplish the conversion but if the focus is narrowed to isolated switch mode power supplies it can be see that that group shares a few basic building blocks, as shown in Fig. 1.

![Fig. 1. Basic isolated switch mode power supply building blocks.](image)

Going forward it has been assumed that the filter, rectifier and the boost stage have already been designed and as these circuits are not the focus of this thesis, their design is not covered.
Moving into specifics let’s look at the building blocks of the fixed frequency resonant converter power supply as seen in Fig. 2 where there are two converters, a transformer, a regulator and a feedback loop.

The boost converter takes the rectified AC voltage and turns it into a DC voltage and the push-pull converter switches that DC voltage through the transformer to get a stepped down voltage on the secondary side. The Buck regulator provides output voltage regulation and current limiting.

The active clamp forward converter, which is an adaptation of the forward converter, takes the place of the old push-pull converter and the synchronous rectification stage replaces the synchronous Buck regulation, the resulting configuration can be seen in Fig. 3. The assumption in further theory is that the active clamp converter has a DC input voltage.

---

**Fig. 2. Fixed frequency resonant converter building blocks.**

**Fig. 3. Building blocks of the Active Clamp Forward Converter.**
A generic low-side active clamp converter with free wheeling synchronous rectification can be seen in Fig. 4, where $L_{\text{leakage}}$ and $L_{\text{mag}}$ is the leakage inductance and magnetizing inductance of the transformer respectively and $C_{\text{par}}$ is the parasitic capacitance of the main MOSFET, $\text{TR}_{\text{main}}$. In the design proposed there is one free wheeling MOSFET and one driven MOSFET but the theory remains the same. A more in depth analysis of the currents, voltages and timings involved in this design can be found in [1] but the general idea is shown in Fig. 5 and the timings are described below.

Fig. 4. Generic low-side active clamp with free wheeling synchronous rectification configuration.

Fig. 5. Primary side switching voltage and drive signals of the low-side active clamp converter.
At time $t_0$ the main voltage $V_{IN}$ is on and the drive signals off, making the switching voltage rise to $V_{IN}$.

At $t_1$ the main drive signal turns on, turning on the TRmain MOSFET and shorting the switching voltage to 0V. The current is now flowing clockwise in the primary side, through the MOSFET.

At $t_2$ the main drive signal turns off, turning off the TRmain MOSFET, but the current continues to flow in the same direction now charging $C_{par}$ up till the voltage has reached $V_{IN}$ level and the capacitance is fully charged. The body diode of the clamp MOSFET, TRclamp, then starts conducting and the current starts charging the clamp capacitor $C_{clamp}$ until the switching voltage has reached $V_{IN}/(1 - D)$, where $D$ is the duty ratio of the TRmain drive signal.

At $t_3$ the clamp drive signal turns on and so turns on TRclamp. This means the switching voltage stops being clamped to $V_{IN}/(1 - D)$ and magnetizing energy starts to charge the clamp capacitor. Half way into the on time of the clamp MOSFET the magnetizing current will reverse direction and start going anti-clockwise as the inductance and capacitance have fully charged and now starts to discharge.

At $t_4$ the clamp drive signal turns back off and with it the clamp MOSFET TRclamp. This means the switching voltage again initially is clamped to $V_{IN}/(1 - D)$ and the current starts flowing through $C_{par}$, discharging the leakage and magnetizing inductances. When these are fully discharged the switching voltage is equal to 0V.

At $t_5$ the main MOSFET TRmain turns on again and the cycle starts over from time $t_1$. 


2.1.1 Design specifications and efficiency

The existing power supply has an input voltage of 115 VAC with a frequency range between 360 Hz and 800 Hz. The turn-on voltage is 94 VAC ± 2 VAC and the turn-off voltage is 86 VAC ± 2 VAC. The turn-off voltage of 86 VAC and the nominal input voltage of 115 VAC translates to a boost voltage turn-off and nominal voltage of 160 VDC and 320 VDC respectively.

The internal clock frequency is set to 200 kHz. The internal frequency sets the speed at which the main control chip runs at.

The output voltage of the existing power supply is +12 VDC with regulation ± 2%, ripple (@ 1 MHz) and noise (@200 MHz) of 2% peak to peak at 8.0 A, a current limit of 10.4 A, and load conditions as stated in Table 1.

<table>
<thead>
<tr>
<th>Operational Load Conditions</th>
<th>Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Load</td>
<td>+12 V - 0.75 A</td>
</tr>
<tr>
<td>Idle Load</td>
<td>+12 V - 1.50 A</td>
</tr>
<tr>
<td>Nominal Load</td>
<td>+12 V - 6.30 A</td>
</tr>
<tr>
<td>Maximum Load</td>
<td>+1 2V - 8.00 A</td>
</tr>
</tbody>
</table>

The efficiency is rated to ≥80%. Efficiency is calculated as the quotient of the output voltage multiplied by the output current divided by the input voltage multiplied by the input current, see Eq. (1).

\[
\text{Efficiency} = \frac{V_{\text{out}} \cdot I_{\text{out}}}{V_{\text{in}} \cdot I_{\text{in}}}
\]  

(1)

Voltages are measured as close to the power supply input and output connections as possible and current is measured as a voltage drop over a sense resistor with a known value in series with the input or output return see Fig. 6.
The efficiency of the active clamp forward converter is measured in the same way although here we have 320 VDC on the input.

![Efficiency measurement of existing power supply.](image)

### 2.2 Transformer Design Basics

The theory of magnetics are extensive and well beyond the scope of this thesis. The purpose of the transformer in a switch mode power supply is for isolation between the primary and secondary but also to step up or down the voltage from primary to secondary. In an ideal transformer the input power equals the output power, this is not the case in reality though. In a real transformer there are a number of loss factors but the major, and often the only, two that are taken into account are **copper losses** and **core losses**. **Copper losses** are losses due to heat buildup in the transformer winding as a result of wire resistance and this changes with the load condition. At light load the loss is less and at higher load the losses are greater, the losses can be calculated as

\[ P_{\text{copper}} = I^2R_{\text{winding}} \]  

where \( P_{\text{copper}} \) is copper loss in watts, \( I \) is the total current going through the transformer in ampere and \( R_{\text{winding}} \) is the wire resistance of both primary and secondary windings of the transformer in ohms.

**Core losses**, which are constant, are losses mainly due to a combination of **hysteresis losses**, losses due to magnetizing inductance and **Eddy current losses**, losses due to induced current as a result of magnetic core flux variations.

In designing a transformer for a specific application the copper losses and core losses must be balanced to minimize the overall power loss. However this does not mean that they as a rule should be the same. \( P_{\text{copper}} \neq P_{\text{core}} \) for most switch mode power supplies.
3 Process and result

3.1 Active clamp PWM controller

The design of the single ended active clamp forward converter was based around the LM5027A chip which is a voltage mode active clamp controller. The decision in using this particular chip was that it was financially viable and also restricted in its maximum duty cycle to 70%. The LM5027A is the chip that gives the main MOSFET, clamp MOSFET and the synchronous MOSFET their drive signals but it also sports features like; overvoltage protection, undervoltage lockout and soft start.

3.1.1 LM5027A functional overview

The LM5027A is a Voltage Mode Active Clamp Controller and main control component of the primary side circuit. The LM5027A is an integrated circuit that supplies the switching signals, and their duty cycle to the clamp (OUTB), the main (OUTA) and the synchronous rectification (OUTSR) MOSFETs.

When powering up the overall electrical circuit the LM5027A output signals are disabled until the voltage on the VCC pin reaches 9.5 V, the internal voltage reference reaches 5 V, the UVLO pin voltage is greater than 2 V, and the OTP pin voltage is greater than 1.25 V. The LM50247A is now in the start-up mode and initializes a soft-start sequence. As a first step in the soft-start sequence the soft-start pins external capacitor is charged by an internal current source raising the voltage on the soft-start pin. As this pin voltage reaches 1.0 V the OUTA (main primary side) and OUTB (primary side clamp) drive signals start switching with an increasing duty cycle. The soft-start pin voltage continues to rise towards its final level of 5 V and as it reaches 4 V the external capacitor on the soft-start synchronous rectification (SSSR) pin starts charging by an internal current source. The voltage on the SSSR pin starts increasing and as it reaches 2.5 V the OUTSR (secondary side synchronous rectification) drive signal is enabled and starts switching with increasing duty cycle. When the soft-start and SSSR pin voltages both have reached 5 V the soft-start sequence is over and normal operation begins.

Under normal operation the duty cycle of the OUTA, OUTB and OUTSR switching drive signals are controlled by the input on the COMP pin, where the drive signals have maximum duty cycle at zero input current and zero duty cycle at 1 mA. The switching drive signals will then stay enabled, with variable duty cycle, unless one of the
following events occurs; the VCC pin voltage falls below 6.0 V, the line undervoltage lockout (UVLO) pin voltage falls below 2.0 V, the over-temperature protection (OTP) pin voltage falls below 1.25 V or the feed-forward modulation ramp (RAMP) pin voltage exceeds 2.5 V.

### 3.2 Main Design

Starting the main design and looking at the LM5027A, a connection diagram taken from the LM5027A datasheet can be seen in Fig. 7 and the setup of the chip and surrounding components will be described here pin by pin.

![LM5027A Pinout](image)

*Fig. 7. LM5027A Pinout. [2]*

**Pin 1 - VIN**

This is the input to the startup regulator and the range is 13 VDC to 90 VDC. As the design has an input of up to 320 VDC and the LM5027A has the ability to be driven solely with the VCC powered, this pin was left unconnected.

**Pin 2 - RAMP**

The RAMP, or feed-forward modulation ramp, gives the LM5027A information about changes in the input voltage before they appear on the output so that the feedback loop, looking at the output voltage, only needs to make small corrections. The ramp amplitude, which increases with decreasing input voltage amplitude, is set by resistor $R_{FF}$ and capacitor $C_{FF}$ connected to the Ramp pin on the IC. The maximum duty cycle, $D_{max}$ was set to $\frac{2}{3}$ and as the switching frequency, $f_{sw} = 200$ kHz and the value of the lowline voltage, $V_{IN,low} = 160$ V, is known from the specifications of the existing power
supply, the values of $R_{FF}$ and $C_{FF}$ can be calculated using the following equation where $V_{ref} = 2.5$ V and noting that the value of $C_{FF}$ should not be below 100 pF nor above 1000 pF, see [2][3].

Note: Initially the $R_{FF}$ value was misread from the calculations and three 47 kΩ resistors were erroneously used in the schematic, see Appendix A, the value of the resistors were changed as a part of the commissioning phase, subsection 3.5, to the correct value of 470 kΩ.

\[
\begin{align*}
    t_{on} &= D_{max} \cdot \frac{1}{f_c} = \frac{2}{3} \cdot \frac{1}{200000} \\
    R_{FF} \cdot C_{FF} &= \frac{V_{IN} \cdot t_{on}}{V_{ref}} \\
    R_{FF} \cdot C_{FF} &= \frac{160 \cdot \frac{2}{3} \cdot \frac{1}{200000}}{2.5} \\
    R_{FF} \cdot C_{FF} &= \frac{2}{9375} \\
\end{align*}
\]

The $R_{FF}$ value is chosen with E24 values in mind and also that it is a high voltage connection so three 1206 package resistors in series were needed. As always the power loss needs to be taken into account and so using the highest value possible without making $C_{FF}$ too small.

\[
    R_{FF} = 470 \text{kΩ} \cdot 3 = 1.41 \text{ MΩ}
\]

\[
    C_{FF} = \frac{\frac{2}{9375}}{1.41 \cdot 10^6} \\
    C_{FF} \approx 151.3 \text{ pF}
\]

Using E24 values adjusts $C_{FF}$ to 150 pF and the maximum power loss in the $R_{FF}$ chain is then calculated as seen in Eq. (10).

\[
    P_{loss} = \frac{320^2}{470 \text{kΩ} \cdot 3} \approx 73 \text{ mW}
\]
Pin 3 - TIME3
The external resistance on this pin sets the delay between the time when the main MOSFET is turned off and the clamp MOSFET is turned on. Using the appropriate graph in [2], initially this was set to approximately 75 ns by a 24 kΩ 0603 package resistor but this was changed to a 62 kΩ resistor in the build stage giving a delay of approximately 200 ns.

Pin 4 - TIME2
The external resistance on this pin sets the delay between the time when the main MOSFET is turned off and the synchronous MOSFET is turned on. Using the appropriate graph in [2], initially this was set to approximately 100 ns by a 33 kΩ 0603 package resistor but this was changed to a 56 kΩ resistor in the build stage giving a delay of approximately 200 ns.

Pin 5 - TIME1
The external resistance on this pin sets the delay between the time when the clamp MOSFET is turned off and the main MOSFET is turned on, it also sets the maximum duty cycle calculated by Eq. (11) where 0.72 is the internally restricted 72% maximum duty cycle for the LM5027A. Using the appropriate graph in [2] the delay $T_1$ was set to approximately 270 ns by a 56 kΩ and a 27 kΩ 0603 package resistor in series giving a maximum duty cycle of 66%.

\[
\text{Max Duty Cycle} = \frac{0.72 \cdot \frac{1}{f_{sw}} - T_1}{\frac{1}{f_{sw}}}
\]  

(11)

Pin 6 - AGND
Analog ground. This is connected straight to power ground PGND.

Pin 7 - RT
RT or oscillator frequency control and sync clock input sets the internal oscillator. A resistor between the pin and ground sets the fundamental frequency and though this resistor is essential, an external pulse can be used to sync the LM5027A to an external source providing that that pulse frequency is at least 10% higher than the frequency set by the resistor. Initially this pin was connected to an arbitrary function generator via a 100 pF capacitor running at a frequency of 200 kHz and the fundamental frequency was set to 150 kHz by one 56 kΩ and one 24 kΩ resistor. This was changed during the
commissioning phase and the frequency $f_{sw}$ was set to 200 kHz by a resistor at a value calculated by Eq. (12), found in [2].

$$R_{RT} = \frac{1}{f_{sw} \cdot 8.3567 \cdot 10^{-11}}$$

\textit{Pin 8 - COMP}
This is the input pin to the pulse width modulator inside the chip and here is where the result from the secondary side feed-back loop is fed. To get an isolated secondary side the feedback circuit is connected to an optocoupler and the other end of the optocoupler is connected to the COMP pin, as the current through the optocoupler to the pin goes from zero up to 1 mA the PWM duty cycle goes from maximum to zero. As the drive signals are based on the PWM they will also change with the increasing or decreasing current from the feedback loop. This means that the drive signal duty cycle can adjust to load changes or input voltage changes.

\textit{Pin 9 - REF}
A 5 VDC output, this is decoupled with a 100 nF capacitor to ground, initially this capacitor was overlooked but was added during the commissioning phase. The optocoupler mentioned in the previous section is powered from this pin.

\textit{Pin 10 - OUTB}
The output on this pin is the clamped P-channel MOSFET drive signal. It was decided to put in an external buffer for this signal, partly to suppress any noise on the signal due to the switching of the MOSFET but also as it was unsure if the LM5027A could source enough current to drive the MOSFET.

\textit{Pin 11 - OUTA}
The output on this pin is the main N-channel MOSFET drive signal. As for the OUTB pin it was decided to put in an external buffer for this signal, partly to suppress any noise on the signal due to the switching of the MOSFET but also as it was unsure if the LM5027A could source enough current to drive the MOSFET.

\textit{Pin 12 - OUTSR}
The output on this pin is the secondary side synchronous N-channel MOSFET drive signal.
**Pin 13 - PGND**

Power ground. Connected to analog ground \( AGND \)

**Pin 14 - VCC**

As \( VIN \) is not connected, this pin serves as the input power pin for driving the chip connected via a RC-network to the 12 V rail \( VAUXP \). The RC-network consists of a 10 \( \Omega \) resistor and a 100 nF capacitor.

**Pin 15 - CS**

Current sense input. An overcurrent state occurs when the voltage on this pin reaches 500 mV. To isolate the current for measurement a 100:1 current transformer was used. The value of the sense resistor was dependent on the current amplitude the overcurrent state should trip at and this would be just over the sum of the max load current, the magnetizing current, the current through the inductance on the secondary side and stray leakage currents. The max load current was set to 10.4 A, the same as the existing power supply and the secondary side inductance current was calculated in Eq. (15).

\[
t_{D_{max}} = D_{max} \cdot \frac{1}{f_{sw}}
\]  

\[
t_{D_{max}} = 2 \cdot \frac{1}{3} \cdot \frac{1}{200 \text{ kHz}}
\]  

\[
I_{L_{curr}} = \frac{V_{OUT} \cdot t_{D_{max}}}{L_{L2}}
\]  

\[
I_{L_{curr}} = \frac{12V \cdot \left( \frac{2}{3} \cdot \frac{1}{200 \text{ kHz}} \right)}{36 \mu\text{H}}
\]

As these are both secondary side currents they have to be scaled twice, from secondary to primary side and then again over the current transformer, resulting in 12.95 mA at the current sense pin. To account for the magnetizing current and stray leakage currents the overcurrent state was set to 20 mA. This in turn sets the sense resistor value to 25 \( \Omega \) but a 24 \( \Omega \) resistor was chosen as it was easily available. An RC-network was also connected to the CS pin, this to stop the LM5027A going into over current due to spikes, transients or noise. A time constant of 50 ns was chosen and the resistor chosen to 100 \( \Omega \) making the theoretical capacitance 500 pF but 470 pF was used as it was the closest E24 value easily available. A diode was also put in in series with
the decoupling resistor to suppress negative voltage on the CS pin.

Note: Initially the capacitance was miscalculated to 75 \text{ pF} and the secondary side connections on the transformer were switched, both errors were discovered and corrected during the commissioning phase.

**Pin 16 - SS**

Soft start pin. When this pin reaches between 1 V to 3 V the main drive signal, OUTA, and the clamp drive signal, OUTB, are enabled and OUTA then increases with the voltage on the SS pin. This pin has an internal current source of 22 \text{ \mu A}, I_{SS}, that charges the external capacitor, \( C_{SS} \), where the value of the capacitor sets the time between the voltage being applied to VCC and the SS pin reaching 3 V. An initial value of 5 ms, \( t_{SS} \), was decided for the soft start and the value of the capacitor can be seen calculated in Eq. (17). This was miscalculated to 33 \text{ nF} but as the time difference with this erroneous value only was 100 \text{ \mu s} the 33 \text{ nF} value was used.

\[
C_{SS} = \frac{I_{SS} \cdot 5 \text{ ms}}{3 \text{ V}}
\]  
Eq. (17)

\[
C_{SS} \approx 36 \text{ nF}
\]  
Eq. (18)

**Pin 17 - RES**

Restart timer, or current limit restart timer pin. If an overcurrent condition is detected on the CS pin an internal 22 \text{ \mu A} current source on the RES pin is enabled and the external capacitor \( C_{RES} \) on the RES pin charges up. The value of the \( C_{RES} \) capacitor decides how many times an overcurrent condition can take place, in a row, before the RES pin voltage reaches 1 V and a hiccup mode ensues \[2\]. If no overcurrent condition occurs a 5 \text{ \mu A} current sink discharges the \( C_{RES} \) capacitor and the RES pin gets tied to ground. As this feature needed to be adjusted to suit the application an initial value of 47 \text{ nF}, suggested by \[3\] was chosen.

**Pin 18 - SSSR**

Soft start for synchronous rectifier output. This is a part of the soft start for the power supply. As the voltage on the soft start pin reaches 4 V the internal 25 \text{ \mu A} current source is enabled and starts charging the external \( C_{SSSR} \) capacitor. When the voltage on the SSSR pin reaches approximately 2.5 V the synchronous drive signal, OUTSR, is enabled and increases with the rising voltage on the SSSR pin. According to the specifications
of the fixed frequency resonant power supply the main output of the unit should have a rise time between 5 ms and 20 ms. This rise time is set with the value of the capacitor externally connected to the SSSR pin and the value is calculated with Eq. (19), giving a rise time to 12.5 ms, \( t_{SSSR} = 12.5 \) ms.

\[
C_{SSSR} = \frac{I_{SSSR} \cdot t_{SSSR}}{V_{SSSR}} \tag{19}
\]

\[
C_{SSSR} = \frac{25 \cdot 10^6 \cdot 12.5 \cdot 10^{-3}}{2} \tag{20}
\]

\[
C_{SSSR} = 156 \ \text{nF} \tag{21}
\]

Using E24 values adjusts the capacitance to \( C_{SSSR} \approx 150 \ \text{nF} \) and the adjusted rise time becomes 12 ms.

**Pin 19 - OTP**

Over temperature protection pin. This pin was not needed as the existing power supply already has an over temperature circuit and was pulled up to the REF pin via a 10 kΩ resistor as to not induce an erroneous over-temperature condition.

**Pin 20 - UVLO**

Line undervoltage lockout. An external voltage divider sets the limits on turn-off and turn-on input voltage where the total resistance is calculated according to Eq. (22) and the calculation for \( R_2 \) in the voltage divider can be seen in Eq. (23) [2]. An extra resistor, \( R_3 \), is put in line with the UVLO pin to facilitate adjustment and the calculation for this resistor can be seen in Eq. (28). The UVLO has an internal 20 µA current sink, \( I_{hys} = 20 \) µA, that provides hysteresis as the voltage on the pin exceeds 2 V.

As the specifications for the existing power supply state that the unit should turn off when the boost voltage falls below 160 V, \( V_{PWR} = 160 \) V, this must be the 2 V equivalent, \( V_{thr} = 2.0 \) V, as the internal comparator turns the unit off when the voltage on the UVLO pin goes below 2 V. As the turn on boost voltage as per specifications should be 250 V the equivalent comparator voltage is 3.125 V and the hysteresis voltage is then 3.125 V - 2 V = 1.125 V, \( V_{HYS} = 1.125 \) V.

\[
R_{tot} = \frac{V_{HYS}}{I_{hys}} \tag{22}
\]
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\[ R_2 = \frac{V_{thr} \cdot R_1}{V_{PW} - V_{thr} - I_{hys} \cdot R_1} \]  

(23)

\[ R_{tot} = \frac{1.125}{20 \cdot 10^{-6}} \]  

(24)

\[ R_{tot} = 56250 \, \Omega \]  

(25)

\[ R_{tot} \approx 56 \, k\Omega \]  

(26)

\[ R_{tot} = R_3 + \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} \]  

(27)

Deciding on a high value for \( R_1 \) as to limit power loss and the fact that three 1206 packaged resistors were needed due to the high voltage, \( R_1 = 3 \, M\Omega \) \((1 \, M\Omega \cdot 3)\) was chosen. The value for \( R_2 \) was decided to be 38 k\Omega.

\[ R_3 = R_{tot} - \frac{1}{\frac{1}{R_1} + \frac{1}{R_2}} \approx 18475 \, \Omega \]  

(28)

Adjusting the resistance using E24 values sets \( R_3 \) to 18 k\Omega. A capacitor was also put in to suppress noise and the roll-off frequency was decided to be a tenth of the switching frequency. The capacitance, \( C_{UVLO} \), was calculated to be 142 pF by Eq. (29). Initially this was miscalculated to 330 pF and this has yet to be changed.

\[ C_{UVLO} = \frac{1}{2 \cdot \pi \cdot \frac{L_{sw}}{10} \cdot R_{tot}} \]  

(29)
3.2.1 Feedback loop

Although the secondary side feedback loop was based on an already existing and proven design with a current sense loop inside a voltage sense loop, the different parts of the loop needed to be calculated. The loop gain needs to be as close to 1, unity, as possible at the maximum frequency for the loop since if the loop gain starts moving away from 1 the phase shift of the loop increases its angle and can cause the loop output signal to invert, so this needs to be calculated for any specific design. The different parts of the current loop calculations can be seen in Fig. 8.

\begin{figure}
\centering
\includegraphics[width=\textwidth]{fig8.png}
\caption{Current feedback loop parts.}
\label{fig:feedback-loop}
\end{figure}

Initially the current sense loop was calculated with a ramp resistance, $R_{\text{ramp}}$, value of 220 kΩ and ramp capacitance, $C_{\text{ramp}}$, value of 1 nF, hence initially the current sense loop calculations yielded the following:

$$I_{\text{ramp}} = \frac{V_{\text{IN}}}{R_{\text{ramp}}} = \frac{320 \text{V}}{220 \text{k} \Omega} = 1.45 \text{ mA}$$  \hfill (30)

$$\frac{dv}{dt} = \frac{I_{\text{ramp}}}{C_{\text{ramp}}} = \frac{1.45 \text{ mA}}{1 \text{nF}} = 1.45 \text{ V/\mu s}$$  \hfill (31)

Ramp amp. @320 V = $T \cdot \frac{dv}{dt} = 5 \text{ \mu s} \cdot 1.45 \text{ V/\mu s} = 7.25 \text{ V}$,  \hfill (32)

where $T = \frac{1}{f_{\text{sw}}} = 5 \text{ \mu s}$, $f_{\text{sw}} = 200 \text{ kHz}$ and $V_{\text{IN}} = 320 \text{ V}$. 

17
\[ G_{PWM} = \frac{V_{IN}}{\text{Ramp amp. @320V}} = \frac{320}{7.25} \approx 44.14 \]  

The gain from control voltage to output, \( G_{PW} \) is therefore:

\[ G_{CPWR} = \frac{G_{PWM}}{n} = \frac{44.14}{36} \approx 5 \]  

\[ Z_L = 2 \cdot \pi \cdot f_1 \cdot L = 2 \cdot \pi \cdot 30 \cdot 10^3 \cdot 36 \cdot 10^{-6} \approx 6.8 \Omega \]  

\[ G_{ZL} = \frac{R_{sense}}{Z_L} = \frac{0.005}{6.8} \]  

where \( n = \) transformer turns ratio, \( f_1 = \frac{f_{sw}}{6} \), \( L = 36 \) μH and \( R_{sense} = 5 \) mΩ.

\[ G_{opto} = \frac{R_2}{R_1} = \frac{5 \cdot 10^3}{2.2 \cdot 10^3} \]  

\( R_1 \) is calculated so that the the current on the chip side guarantees the full voltage range. As the minimum current transfer ratio of the optocoupler is 22% an absolute minimum current on the feedback loop side of the optocoupler to guarantee 5 V on the chip side is 4.541 mA, as \( R_2 \) is an internal 5 kΩ resistance of the LM5027A, and the \( R_1 \) value becomes 2.64 kΩ. To get a measure of redundancy \( R_1 \) was chosen to be 2.2 kΩ, roughly half of the internal resistance.

\[ G_{ZL} \cdot G_{CEA} \cdot G_{opto} \cdot G_{PW} = 1 \]  

\[ \frac{R_f}{R_{in}} = G_{CEA} - 1 = \frac{1}{G_{ZL} \cdot G_{opto} \cdot G_{CPWR}} - 1 \approx 120 \]  

\[ R_{in} = \frac{R_f}{120} = \frac{180 \cdot 10^3}{120} = 1.5 \text{ kΩ} \]
The voltage loop is similarly calculated and the parts can be seen in Fig. 9.

\[ G_{V\text{PWR}} = \frac{1}{R_{\text{sense}}} \] (41)

\[ G_{ZC} = Z_o = \frac{1}{2 \cdot \pi \cdot f_2 \cdot C_o} \] (42)

\[ G_V = \frac{V_{\text{ref}}}{V_{\text{out}}} \] (43)

\[ V_{\text{smax}} = R_{\text{sense}} \cdot I_{\text{current \_ limit}} \] (44)

\[ G_R = \frac{R_5}{R_6} = \frac{V_{\text{ref}}}{V_{\text{smax}}} \] (45)

\[ G_{V\text{PWR}} \cdot G_{ZC} \cdot G_V \cdot G_R \cdot G_{V\text{EA}} = 1 \] (46)

\[ G_{V\text{EA}} = \frac{V_{\text{out}} \cdot R_5}{Z_c \cdot R_6 \cdot V_{\text{ref}} \cdot G_{V\text{PWR}}} \] (47)

\[ \frac{R_3}{R_4} = G_{V\text{EA}} - 1 \] (48)
As a rule of thumb the capacitors $C_o$, $C_{zc}$, $C_{zv}$ and $C_{pv}$ are calculated as follows,

\[
C_o = \frac{1}{2 \cdot \pi \cdot f_2 \cdot R_f},
\]

\[
C_{zc} = \frac{1}{2 \cdot \pi \cdot f_{zc} \cdot R_f},
\]

\[
C_{zv} = \frac{1}{2 \cdot \pi \cdot f_{zv} \cdot R_3},
\]

\[
C_{pv} = \frac{1}{2 \cdot \pi \cdot f_{pv} \cdot R_3},
\]

where $R_6 = R_{in}$, $f_2 = \frac{f_4}{4} = 6$ kHz, $C_z = 361.1 \mu F$, $V_{ref} = 5$ V, $V_{out} = 12$ V, $I_{current,limit} = 10.4$ A, $f_{zv} = \frac{f_2}{4}$, $f_{pv} = f_2 \cdot 4$ and $f_{zc} = \frac{f_1}{4}$.

Here $R_5$ has the theoretical value of 144 kΩ, the closest E24 value being 150 kΩ. Setting $R_3$ to 20 kΩ gave $R_4$ the value of 1.3 kΩ. As $C_o$ was decided without consideration of $R_3$ and $C_{zv}$ and $C_{pv}$ were calculated based on $f_1$ instead of $f_2$, $C_o$, $C_z$ and $C_o$ were given erroneous values.

### 3.3 Transformer design

As the effective power of the new design and the existing power supply should be the same, the same type of core, RM10, was also used. The material of the core, 3F3, was chosen to be suited for the switching frequency, 200 kHz, with reference to [4]. The base turns ratio was 320:36 since 36 V was needed on the secondary side as the primary duty cycle was 33%. Using empirical tables with values experimentally confirmed, a turns ratio of 42:5 between the primary and the load bearing secondary windings was decided on. It was also decided to start with an ungapped 3F3 core to be able to adjust the gap as needed. Simulations indicated that the primary inductance $L_p$ should be 500 $\mu$H and the relationship between the primary inductance and the AL value, an inductance value of a core that the manufacturers specifies, can be seen in Eq. (53), where $N_p$ is the number of primary turns.

\[
L_p = N_p^2 \cdot A_L
\]

This gives a $A_L$ inductance of 283 nH where the closest gapped value [4] is an $A_L$ inductance of 315 nH and has an air gap of 0.43 mm. To duplicate this with an ungapped
core, three layers of 0.07 mm thick kapton tape were put on the center tap and the legs of one half of the core. The winding layers of the transformer were made up as seen in Fig. 10. Initially the sixth layer was made up of five turns but as this would have given a gate voltage of up to 36 V this winding was cut and a new two turn winding was put on outside the tenth layer.

![Fig. 10. Transformer winding layers.](image)

1st layer consists of 21 turns of 0.4 mm diameter insulated copper wire, this being half the primary winding.

2nd and 3rd layer consist of 0.07 mm thick kapton tape.

4th layer consists of the load bearing secondary winding, five turns of 19 times 0.25 mm diameter insulated copper wire.

5th layer is another layer of kapton tape.

6th layer consists of the two turns 0.1 mm diameter copper wire that gives the free-wheeling synchronous MOSFETs their gate voltage.

7th layer is another layer of kapton tape.

8th layer is the second half of the primary winding, 21 turns of 0.4 mm diameter copper wire.

9th and 10th layer finish the transformer off with two turns of kapton tape.

### 3.4 PCB design

The schematic and PCB layout was done with the Eagle Cad software and the PCB was manufactured outside the company.
3.5 Commissioning

To be able to more easily fault find the design it was built in stages, where the first stage was populating the PCB with the LM5027A and related components to make sure that the calculations resulting in the resistor and capacitor values were correct. The first issue found was that there needed to be a capacitor on the reference pin on the LM5027A as without it there was 2 V of ripple on the 5 V reference voltage. Furthermore the calculations for the resistor values giving the dead space between drive signals were off by as much as 10%.

<table>
<thead>
<tr>
<th>Drive</th>
<th>Resistor value</th>
<th>Calculated time</th>
<th>Measured time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time1</td>
<td>83 kΩ</td>
<td>250 ns</td>
<td>270 ns</td>
</tr>
<tr>
<td>Time2</td>
<td>33 kΩ</td>
<td>100 ns</td>
<td>110 ns</td>
</tr>
<tr>
<td>Time3</td>
<td>24 kΩ</td>
<td>72 ns</td>
<td>72 ns</td>
</tr>
</tbody>
</table>

Deciding that an overall delay of 200 ns was prudent in the initial stage of powering up the design the resistor values of drives Time2 and Time3 was changed to 56 kΩ and 62 kΩ respectively.

Trying to synchronize the oscillator with an external pulse supplied by an arbitrary function generator, the realization was that the LM5027A needed a 15-150 ns wide pulse where the existing power supply gives a pulse of 50% duty cycle at 200 kHz. A design to correct this was suggested, see Fig. 11, but not implemented as the design would give a pulse that momentarily goes 2 V negative and according to [2] no pin should be taken under -0.3 V (referenced to ground). An arbitrary function generator was used as a temporary measure and the issue was left until a later date.

![Fig. 11. Suggested circuit for external oscillator synchronization.](image-url)
Having put in the drive buffers on the primary side a 130 ns time delay between the OUTB drive signal going high and the OUTSR drive signal going low was noticed and as these two instances should be simultaneous the OUTA and OUTB signal buffers were removed.

Going over the schematic, \( R_{34} \) in the feedback circuit was changed from a value of 1.6 kΩ to 150 kΩ to match \( R_{37} \), had it not been changed it would have led to instabilities in the feedback circuit and thus to an instability in the whole design.

At this stage the primary side MOSFETs were fitted and as a help to faultfinding two diodes were fitted on the secondary side instead of the synchronous MOSFETs so as to leave the synchronous rectification out of the primary side and feedback loop functionality. Populating the primary side MOSFETs it was seen that the OUTB drive signal was not switching at 200 kHz but rather at a random frequency. This was found to be due to the external signal generator picking up noise and upsetting the timings. The signal generator was removed and it was decided to hardwire the oscillator by setting the \( R_T \) resistor to give a 200 kHz oscillation, see Eq. (12) page 11. Using E24 values the total resistance was set to 60 kΩ which gives a frequency of 199440 Hz. After this change the frequency of the drive signals was steady.

Looking at the switching voltage at this stage a significant resonant hump was seen and as this was due to the clamp capacitance being too low the value of this component was changed from 2.2 nF to 22.2 nF and a reduction in the resonant voltage could be seen. The design at this stage was unstable and as a help in faultfinding a potentiometer was put in parallel with the soft start capacitor as this would take control of the pulse width of the main drive signal, OUTA, and so control the output of the design. Care was taken in supplying the LM5027A and external parts with enough voltage to overcome startup conditions and make sure that the drive signals would be enabled. Slowly increasing the voltage on the soft start pin from 1 V but not high enough to get 12 V on the output, the main MOSFET failed. To try to rectify this problem, as the cause was unclear, the drive buffers were put back in but with a change in the RC-network, making \( R_{46} \) and \( R_{47} \) 1 kΩ resistors and \( C_{29} \) and \( C_{30} \) 27 pF, so the propagation delay would be smaller. Powering up with this modification broke both the main MOSFET and the clamp MOSFET. After some investigation it was decided to put in a RCD clamp instead of the P-channel clamp MOSFET and the clamp capacitor to simplify fault finding, this lead to a realization that under light load, 0.6 A, the turn on time for the main MOSFET was
approximately 1.5 µs due to the high capacitance of the high voltage rated part, and as the fixed dead space was set to 200 ns this meant that both primary side MOSFETs were on at the same time, which is what caused them to break. At the same time it was seen that the feedback circuit was unstable and the components $C_{35}$ and $R_{49}$ were populated with a 2.2 nF capacitor and a 750 Ω resistor respectively thus creating an RC-network to counter the probable delay in the optocoupler. This helped but instability was still seen and decoupling was put in on the incoming Vaux 12 V and the Vref signal. The suggested fix to the problem of both the main MOSFET and the clamp MOSFET being on at the same time was to put in an adaptive drive timing circuit in the manner shown in Fig. 12. This would disable the drive signal unless the switch voltage was below the input voltage, thus preventing the primary MOSFETs from being on simultaneously. This was implemented on a jockey PCB connected to the main PCB via wiring.

In conjunction with this redesign, research indicated that an RC-network was required in parallel with the clamp capacitor to keep the switching voltage from oscillating so this was implemented with the following equations, given in [6] and seen here, giving the value for the respective component,

$$C_{\text{clamp}} = \frac{1}{2 \cdot L_{\text{mag}}} \cdot \left( \frac{4}{2 \cdot \pi \cdot f_{sw}} \right)$$

(54)
\[
C_{rc} = 6 \cdot C_{clamp} \tag{55}
\]
\[
R_{rc} = \frac{1}{1 - \left(\frac{V_{out}}{V_{in(l)}}, \frac{N_p}{N_s}\right) \sqrt{L_{mag}/C_{clamp}}} \tag{56}
\]

where \( L_{mag} = 580 \) \( \mu \)H, \( f_{ss} = 200 \) kHz, \( V_{out} = 12 \) V, \( V_{in(l)} = 160 \) V, \( N_p = 42 \) and \( N_s = 5 \).

Another thought was also that the design, with the potentiometer turned down low, started in a worst case scenario with short drive pulses and light load. To rectify this the potentiometer was turned up until the pulse width of the drive signal was 20% of the maximum, maximum being 2 \( \mu \)s, so the pulse width was set to 400 ns.

When powering up after these changes two things were noticed, first the pulse width was only 20 ns and secondly the main drive signal only happened every fifth cycle, so instead of the switching frequency being 200 kHz it was 40 kHz. Reexamining the design it was noticed that the RC-network capacitor for the current sense signal, \( C_{15} \), was miscalculated and was corrected to 470 pF, though unfortunately this had no effect.

Changing the clamp MOSFET from the IXTR32P60P to the IXTH10P60 only sped up the switching of the switching voltage, it did nothing to improve the main drive signal problem. Increasing the capacitance of \( C_{15} \) to 1.1 nF finally made the drive signal appear every cycle but the 20 ns pulse width was still a problem. The thought here was that this probably had been the problem all along and that it most probably was due to noise on one of the LM5027A pins. As the correct drive signal had been seen when the power stage was unconnected the way forward was to cut the power tracking between the control and the power stage, letting the control run with 270 V while running the power stage with an increasing voltage, starting at 0 V, to see where the LM5027A lost control.

The power stage was seen to lose control at around 180 V as main drive pulses were suddenly dropped, at first it was thought that this was due to a grounding issue and the connection between the power ground and the control ground was re-tracked. This made no difference. Leaving this change in, the drain of the clamp MOSFET was also re-tracked and after this the DC power supply feeding the power stage went into current limit, 0.5 A, whether this was due to the re-tracking of the drain was uncertain. After changing the gate capacitor \( C_8 \) and the gate diode \( D_5 \) it was noticed that it had no
impact on the problem so the re-tracking was removed and the old clamp MOSFET, IXTR32P60P, was put back in. This put the power stage back to working to the point that it was still loosing control but now at 140 V. The next thing to do was to short out the current transformer, $T_2$, by populating $R_{44}$ with a 0 Ω resistor. Again nothing changed but this gave the thought that the adaptive drive timing circuit was partly running off the 270 V control voltage and partly running with a varied voltage from the power stage and that this might cause the issue. Rewiring the $V_{in}$ connection on the adaptive time drive jockey PCB to the power stage the first problem encountered was that the comparator latched high at startup. Taking the feedback resistor out caused the comparator output to oscillate so a capacitor was put in series with the feedback resistor, the thought being that the capacitor would force the feedback to act as a open circuit just at startup, this again caused the comparator to latch high. The problem was finally solved using a 1 MΩ feedback resistor. It was then noticed that not all the pulses from the comparator reached the AND gate, this was due to a pin on the inverter not properly soldered and after re-flowing the problem with dropped main drive pulses was resolved and the primary side was functioning as intended.

Setting the control stage voltage to 255 VDC and increasing the power stage voltage from 0 VDC to 255 VDC, the potentiometer was wound up to where the LM5027A took control of the main drive signals pulse width to see if the secondary side feedback loop was stable. It was seen that the output voltage gradually reached 11.94 V and as this was an indication of something wrong some of the feedback loop values were changed and at the same time the short on the current transformer was taken off to see if the primary side and the feedback loop on the secondary side would continue stable. This was when it was noticed that the secondary side connections on the current transformer were switched and this was corrected with cutting the tracks and rewiring the connections. After these changes the output was a stable 11.99 V, well within the stated specification.

As the design was now working in regards to the primary side and the feedback loop, the synchronous MOSFETs were to be put in but this meant another buffer needed to be put in on the SR pin signal as this had been overlooked in the original design. This was done while the diodes were still in place as to judge the timings between the synchronous drive signal and the clamp drive signal. When completed the synchronous MOSFETs were put in and when powering up it could be seen that the pulse width of the main drive
signal was minuscule and that the synchronous drive signal was not getting through to the synchronous MOSFET. This was probably a problem with the adaptive drive timing and/or the synchronous drive signal buffer but as the synchronous MOSFETs were put in on the last day of the project there was no more time for fault finding and this was where the design was left.

3.6 Results

The efficiency measured in the new design with diodes instead of the synchronous rectification MOSFETs was 84% in comparison with the existing power supply that has an efficiency of 83%. It should be noted though that for the existing power supply this efficiency figure is for the entire power supply whereas for the new design it’s only for a part of the power supply. In terms of component count the new design uses 160 components with an approximate total price of £22.75, while the existing power supply uses 164 components with a total price of £20.51. The overall comparison can be seen in Table 2 where the actual total size of the components have not been measured but a visual estimate was made and as the synchronous rectification was not implemented the noise and ripple measurements could not accurately be done on the new design.

Table 2. Collated points of comparison.

<table>
<thead>
<tr>
<th>Characteristics for comparison</th>
<th>Existing design</th>
<th>New design</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>83%</td>
<td>84%</td>
<td>New design more efficient</td>
</tr>
<tr>
<td>Number of components</td>
<td>164 pcs</td>
<td>160 pcs</td>
<td>New design has less components</td>
</tr>
<tr>
<td>Size of components</td>
<td>visual estimate</td>
<td>visual estimate</td>
<td>Equal size of total component count</td>
</tr>
<tr>
<td>Noise and ripple</td>
<td>9.08 mV</td>
<td>not measured</td>
<td>unknown</td>
</tr>
<tr>
<td>Cost</td>
<td>£20.51</td>
<td>£22.75</td>
<td>Existing design is cheaper</td>
</tr>
</tbody>
</table>
4 Discussion

The results show that from an economic point of view the low side active clamp forward converter in its current state is not an improvement on the existing power supply. This is mainly due to the P-channel MOSFET which is approximately five times more expensive than an equivalent N-channel MOSFET, and also the added cost of the adaptive drive timing circuit.

Comparing the efficiency is more difficult as the design was never fully realized. It is likely, if the synchronous rectification can be made to work, that the new design will increase in efficiency to the degree where, even including the losses in the rest of the power supply, it will be more efficient than the existing power supply. If so, even offset against the increased relative cost this would make the new design a viable replacement. Going forward, making the synchronous rectification work would be the first thing to do. This would give a much clearer idea of the overall efficiency of the system. Another thing to try to improve efficiency would be to do a price vs capacitance vs $R_{\text{DS(on)}}$ comparison for the main MOSFET as at this time the primary side is still hard switching the MOSFET because of the MOSFET’s slow response due to high capacitance. Unfortunately MOSFETs with low capacitance have a higher $R_{\text{DS(on)}}$ resistance or higher price. So this would be a balancing act, but is worth looking into. An increase in leakage inductance could also be a way of ensuring zero volt switching of the primary side. If zero volt switching is achieved the RC-network on the clamp capacitor could be looked at and possibly removed, again increasing efficiency and lowering the price, although only marginally.

In the event that trying all the above still does not produce a useful design, a final alternative approach would be to make the converter high side driven. The P-channel clamp MOSFET could then be replaced with an N-channel MOSFET which would bring the price down and hopefully the efficiency up. However, this would require a redesign which would undoubtedly come with additional challenges, and so may not be a trivial project.
5 Conclusion

The low side driven active clamp forward converter with synchronous rectification could be a suitable replacement for the existing power supply design, providing improvement of efficiency when the design is fully realized. As the design shows promise it would be worth investing time to complete the prototype to establish its final performance.
References


[2] ”Voltage Mode Active Clamp Controller.” Texas Instruments, Dallas, TX, Datasheet SNVS642B. 2013.


Appendix A
Appendix B